

SYNC MASTER=J13 MLB		SYNC DATE=11/18/2011	
PAGE TITLE			
System Block Diagram		DRAWING NUMBER	051-9276
Apple Inc.		REVISION	2.7.0
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BOM Variants							
BOM NUMBER	BOM NAME	BOM OPTIONS					
639-3469	PCBA,MLB,1.5GHZ,HY 4GB,J11	J11_CMNPTS,CPU:1.5GHZ,EEEE:DYKL,DDR3:HYNIX_4GB					
639-3470	PCBA,MLB,1.5GHZ,SA 4GB,J11	J11_CMNPTS,CPU:1.5GHZ,EEEE:DYKH,DDR3:SAMSUNG_4GB					
639-3473	PCBA,MLB,1.5GHZ,HY 8GB,J11	J11_CMNPTS,CPU:1.5GHZ,EEEE:DYKJ,DDR3:HYNIX_8GB					
639-3659	PCBA,MLB,1.5GHZ,EL 8GB,J11	J11_CMNPTS,CPU:1.5GHZ,EEEE:FOVJ,DDR3:ELPIDA_8GB					
639-3471	PCBA,MLB,1.7GHZ,HY 4GB,J11	J11_CMNPTS,CPU:1.7GHZ,EEEE:DYKL,DDR3:HYNIX_4GB					
639-3472	PCBA,MLB,1.7GHZ,SA 4GB,J11	J11_CMNPTS,CPU:1.7GHZ,EEEE:DYKF,DDR3:SAMSUNG_4GB					
639-3775	PCBA,MLB,1.7GHZ,EL 4GB,J11	J11_CMNPTS,CPU:1.7GHZ,EEEE:F27J,DDR3:ELPIDA_4GB					
639-3474	PCBA,MLB,1.7GHZ,HY 8GB,J11	J11_CMNPTS,CPU:1.7GHZ,EEEE:DYKH,DDR3:HYNIX_8GB					
639-3774	PCBA,MLB,1.7GHZ,SA 8GB,J11	J11_CMNPTS,CPU:1.7GHZ,EEEE:F27D,DDR3:SAMSUNG_8GB					
639-3660	PCBA,MLB,1.7GHZ,EL 8GB,J11	J11_CMNPTS,CPU:1.7GHZ,EEEE:FOV4,DDR3:ELPIDA_8GB					
639-3776	PCBA,MLB,2.0GHZ,HY 4GB,J11	J11_CMNPTS,CPU:2.0GHZ,EEEE:F27K,DDR3:HYNIX_4GB					
639-3778	PCBA,MLB,2.0GHZ,SA 4GB,J11	J11_CMNPTS,CPU:2.0GHZ,EEEE:F27G,DDR3:SAMSUNG_4GB					
639-3780	PCBA,MLB,2.0GHZ,EL 4GB,J11	J11_CMNPTS,CPU:2.0GHZ,EEEE:F27H,DDR3:ELPIDA_4GB					
639-3777	PCBA,MLB,2.0GHZ,HY 8GB,J11	J11_CMNPTS,CPU:2.0GHZ,EEEE:F27C,DDR3:HYNIX_8GB					
639-3779	PCBA,MLB,2.0GHZ,SA 8GB,J11	J11_CMNPTS,CPU:2.0GHZ,EEEE:F27F,DDR3:SAMSUNG_8GB					
639-3781	PCBA,MLB,2.0GHZ,EL 8GB,J11	J11_CMNPTS,CPU:2.0GHZ,EEEE:F279,DDR3:ELPIDA_8GB					
085-3937	J11 MLB DEVELOPMENT BOM	J11_DEVEL-BMG					
607-9089	CMN PTS,PCBA,MLB,J11	J11_CMNPN					
939-0479	PCBA,MLB,1.9GHZ,HY 4GB,J11	J11_CMNPTS,CPU:1.9GHZ,EEEE:DYKL,DDR3:HYNIX_4GB					
Bar Code Labels / EEEE #'s							
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION		
825-7670	1	LABEL,TEXT,MLB,K21/K78	[EEEE_DYKL]	CRITICAL	EEEE:DYKL		
825-7670	1	LABEL,TEXT,MLB,K21/K78	[EEEE_DYKH]	CRITICAL	EEEE:DYKH		
825-7670	1	LABEL,TEXT,MLB,K21/K78	[EEEE_DYKJ]	CRITICAL	EEEE:DYKJ		
825-7670	1	LABEL,TEXT,MLB,K21/K78	[EEEE_DYKF]	CRITICAL	EEEE:DYKF		
825-7670	1	LABEL,TEXT,MLB,K21/K78	[EEEE_DYKJ]	CRITICAL	EEEE:DYKJ		
825-7670	1	LABEL,TEXT,MLB,K21/K78	[EEEE_DYKG]	CRITICAL	EEEE:DYKG		
825-7670	1	LABEL,TEXT,MLB,K21/K78	[EEEE_FOV3]	CRITICAL	EEEE:FOV3		
825-7670	1	LABEL,TEXT,MLB,K21/K78	[EEEE_FOV4]	CRITICAL	EEEE:FOV4		
825-7670	1	LABEL,TEXT,MLB,K21/K78	[EEEE_F279]	CRITICAL	EEEE:F279		
825-7670	1	LABEL,TEXT,MLB,K21/K78	[EEEE_F27C]	CRITICAL	EEEE:F27C		
825-7670	1	LABEL,TEXT,MLB,K21/K78	[EEEE_F27D]	CRITICAL	EEEE:F27D		
825-7670	1	LABEL,TEXT,MLB,K21/K78	[EEEE_F27F]	CRITICAL	EEEE:F27F		
825-7670	1	LABEL,TEXT,MLB,K21/K78	[EEEE_F27G]	CRITICAL	EEEE:F27G		
825-7670	1	LABEL,TEXT,MLB,K21/K78	[EEEE_F27H]	CRITICAL	EEEE:F27H		
825-7670	1	LABEL,TEXT,MLB,K21/K78	[EEEE_F27J]	CRITICAL	EEEE:F27J		
825-7670	1	LABEL,TEXT,MLB,K21/K78	[EEEE_F27K]	CRITICAL	EEEE:F27K		
Sub-BOMs							
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION		
085-3937	1	J11 MLB DEVELOPMENT BOM	DEVEL	CRITICAL	DEVEL_BOM		
607-9089	1	CMN PTS,PCBA,MLB,J11	CMNPTS	CRITICAL	J11_CMNPTS		
K78 BOM Variants							
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J11 BOM GROUPS

BOM GROUP	BOM OPTIONS
J11_COMMON	ALTERNATE,COMMON,J11_MISC,J11_DEBUG:ENG,J11_PROGPARTS,USBHUB2513B,EDP:YES,PCH_C1
J11_MISC	HUB_3NONREM,TBT,MPM5:YES,CPUMEM_SLG:NO,PF5VS_DCIN:NO,TPAD_PCH:NO,SKIP_5V3V3:INAUDIBLE,HTPWR:S4,TBTW:P15V,LVDDR3_HW:YES,AKG_ACOUSTICS:NO
J11_PROGPARTS	BOOTROM_PROG,SMC_PROG,TBTROM:PROG
J11_DEVEL:ENG	ALTERNATE,BKLT:ENG,XDP_CONN,XDP_PCH,DORVREF_SAC,VREFQ0:M3,VREFCA:LDO_DAC,SDQ00D_ISL,S3_S0_LSD,VCCIOISNS_ENG,AIRPORTISNS_ENG,HDDISNS_ENG,LCDCLKTISNS_ENG
J11_DEVEL:PVT	XDP_CONN
J11_DEBUG:ENG	DEVEL_BOM,MOJO:YES,XDP,XDP_CPU:BPM,LPCPLUS
J11_DEBUG:PVT	DEVEL_BOM,BKLT:PROD,MOJO:YES,XDP,LPCPLUS,VREFQ0:LDO,VREFCA:LDO,XDP_CPU:BPM,VCCIOISNS_PROD,AIRPORTISNS_PROD,HDDISNS_PROD,LCDCLKTISNS_PROD
J11_DEBUG:PROD	BKLT:PROD,MOJO:YES,XDP,LPCPLUS,VREFQ0:LDO,VREFCA:LDO,XDP_CPU:BPM,VCCIOISNS_PROD,AIRPORTISNS_PROD,HDDISNS_PROD,LCDCLKTISNS_PROD
DDR3:HYNIX_4GB	RAMCFG0:L,RAMCFG1:L,RAMCFG2:L,RAMCFG3:L,DRAM_TYPE:HYNIX_4GB
DDR3:HYNIX_8GB	RAMCFG0:L,RAMCFG1:L,RAMCFG2:H,RAMCFG3:L,DRAM_TYPE:HYNIX_8GB
DDR3:SAMSUNG_4GB	RAMCFG0:L,RAMCFG1:H,RAMCFG2:L,RAMCFG3:L,DRAM_TYPE:SAMSUNG_4GB
DDR3:SAMSUNG_8GB	RAMCFG0:L,RAMCFG1:H,RAMCFG2:H,RAMCFG3:L,DRAM_TYPE:SAMSUNG_8GB
DDR3:ELPIDA_4GB	RAMCFG0:H,RAMCFG1:H,RAMCFG2:L,RAMCFG3:L,DRAM_TYPE:ELPIDA_4GB
DDR3:ELPIDA_8GB	RAMCFG0:H,RAMCFG1:H,RAMCFG2:H,RAMCFG3:L,DRAM_TYPE:ELPIDA_8GB

Programmable Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
335S0865	1	EEPROM,256KBIT,SPI,5MHZ,1.8V,2K3QFN	U3690	CRITICAL	TOPROM:BLANK
341S3526	1	IC,EEPROM,Cmltius Bridge (V1.2) P18, J11/J13	U3690	CRITICAL	TOPROM:PROG
338S1098	1	IC,SMC12-A3,40MHZ/50KMDP MCU,9X9,157BGA	U4900	CRITICAL	SMC:BLANK
341S3434	1	IC,SMC,P18,J11	U4900	CRITICAL	SMC:PROG
335S0869	1	64 MBIT SPI SERIAL DUAL I/O FLASH,KEE5-4	U6100	CRITICAL	BOOTROM:BLANK
335S0803	1	64 MBIT SPI SERIAL DUAL I/O FLASH,KEE5-8	U6100	CRITICAL	BOOTROM:BLANK
341S3527	1	IC,EFI ROM,P18,J11/J13	U6100	CRITICAL	BOOTROM:PROG

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
37680855	37680613		ALL	Diodes alt to Toshiba
37680977	37680859		ALL	Diodes alt to Toshiba
37680972	37680612		ALL	Kohm alt to Toshiba
13880676	13880691		ALL	Murata alt to Samsung
37180709	37180652		ALL	NEP alt to NEP
13880671	13880673		ALL	Taiyo alt to Murata
15281085	15281307		ALL	Toko alt to Cyntec
15281462	15281295		ALL	Toko alt to NEC Inductor
13880684	13880660		ALL	Murata alt to Taiyo Yuden
13880703	13880648		ALL	Murata alt to Taiyo Yuden
15281493	15281300		ALL	Collofrat: MA5274 alt to Murata
15280586	15281301		ALL	Dale/Vishay alt to Cynotec
35383238	35381428		ALL	Intersil alt to GDA2333
37280186	37280185		ALL	NEP alt to Diodes
19780431	19780432		ALL	200uW Epsom alt to NDK
37681053	37680604		ALL	Diodes alt to Fairchild
37680855	37680613		ALL	Diodes alt to Toshiba
37680903	37680796		ALL	Fairchild alt to Siliconix
37180713	37180558		ALL	Diodes alt to ST Micro
12880333	998-4435		ALL	Sanyo alt to Kemet
12880357	998-4435		ALL	Sanyo High Voltage Polymer alt
998-4715	998-4435		ALL	Kemet Rectangular Design alt
998-4716	998-4435		ALL	Kemet Flute Design alt

DRAM CFG CHART

VENDOR	CFG 1	CFG 0
HYNIX	0	0
SAMSUNG	1	0
MICRON	0	1
ELPIDA	1	1

SIZE	CFG 2
4GB	0
8GB	1

DIE REV	CFG 3
A	0
B	1

Module Parts


PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S4197	1	1VB,Q0P8,RS2,K0,1.5,17W,2+2,0.95,4M,ULVB	U1000	CRITICAL	CPU:1.5GHZ
337S4299	1	1VB,QC98,QS,L1,1.7,17W,2+2,1.05,3M,ULVBG	U1000	CRITICAL	CPU:1.7GHZ
337S4296	1	1VB,QC98,QS,L1,2.0,17W,2+2,1.15,4M,ULVBG	U1000	CRITICAL	CPU:2.0GHZ
337S4198	1	1VB,Q8TP,RS2,K0,1.5,17W,2+2,0.95,4M,ULVBGA	U1000	CRITICAL	CPU:1.5GHZTDP
337S4299	1	1VB,QC98,QS,L1,1.7,17W,2+2,1.05,3M,ULVBG	U1000	CRITICAL	CPU:1.7GHZTDP
337S4296	1	1VB,QC98,QS,L1,2.0,17W,2+2,1.15,4M,ULVBG	U1000	CRITICAL	CPU:2.0GHZTDP
337S4297	1	1VB,QC9C,QS,L1,1.9,17W,2+2,1.15,4M,ULVBG	U1000	CRITICAL	CPU:1.9GHZ
337S4165	1	1C,PCH,PPT-MB,SFF,RS1	U1800	CRITICAL	PCH_RS1
337S4180	1	1C,PCH,PPT-MB,SFF,RS2,B0	U1800	CRITICAL	PCH_RS2
337S4235	1	1C,PCH,PPT-MB,SFF,P-QS,C0	U1800	CRITICAL	PCH_C0
337S4275	1	1C,PCH,PPT-MB,Q877,C1,QS	U1800	CRITICAL	PCH_C1
337S4275	1	1C,PCH,PPT-MB,Q877,C1,QS	U1800	CRITICAL	PCH_C1TDP
338S1108	1	1C,TBT,CR-4C,LP,ES3,288 PCBGA,12X12MM	U3600	CRITICAL	TBT

333S0622	4	IC, SDRAM, 2GBIT, DDR3L-1600, GEMMA, 78P FPGA	U2900, U2910, U2920, U2930	CRITICAL	DRAM_TYPE=HYNIX_4GB
333S0622	4	IC, SDRAM, 2GBIT, DDR3L-1600, GEMMA, 78P FPGA	U3000, U3010, U3020, U3030	CRITICAL	DRAM_TYPE=HYNIX_4GB
333S0622	4	IC, SDRAM, 2GBIT, DDR3L-1600, GEMMA, 78P FPGA	U3100, U3110, U3120, U3130	CRITICAL	DRAM_TYPE=HYNIX_4GB
333S0622	4	IC, SDRAM, 2GBIT, DDR3L-1600, GEMMA, 78P FPGA	U3200, U3210, U3220, U3230	CRITICAL	DRAM_TYPE=HYNIX_4GB
333S0625	4	IC, SDRAM, 4GBIT, 512MK8, DDR3-1600, 82 FBGA	U2900, U2910, U2920, U2930	CRITICAL	DRAM_TYPE=HYNIX_8GB
333S0625	4	IC, SDRAM, 4GBIT, 512MK8, DDR3-1600, 82 FBGA	U3000, U3010, U3020, U3030	CRITICAL	DRAM_TYPE=HYNIX_8GB
333S0625	4	IC, SDRAM, 4GBIT, 512MK8, DDR3-1600, 82 FBGA	U3100, U3110, U3120, U3130	CRITICAL	DRAM_TYPE=HYNIX_8GB
333S0625	4	IC, SDRAM, 4GBIT, 512MK8, DDR3-1600, 82 FBGA	U3200, U3210, U3220, U3230	CRITICAL	DRAM_TYPE=HYNIX_8GB
333S0623	4	IC, SDRAM, 2GBIT, DDR3-1600, D35, 78P FBGA	U2900, U2910, U2920, U2930	CRITICAL	DRAM_TYPE=SAMSUNG_4GB
333S0623	4	IC, SDRAM, 2GBIT, DDR3-1600, D35, 78P FBGA	U3000, U3010, U3020, U3030	CRITICAL	DRAM_TYPE=SAMSUNG_4GB
333S0623	4	IC, SDRAM, 2GBIT, DDR3-1600, D35, 78P FBGA	U3100, U3110, U3120, U3130	CRITICAL	DRAM_TYPE=SAMSUNG_4GB
333S0623	4	IC, SDRAM, 2GBIT, DDR3-1600, D35, 78P FBGA	U3200, U3210, U3220, U3230	CRITICAL	DRAM_TYPE=SAMSUNG_4GB
333S0642	4	IC, SDRAM, 4GBIT, DDR3-1600, C-DIE, 78P FBGA	U2900, U2910, U2920, U2930	CRITICAL	DRAM_TYPE=SAMSUNG_8GB
333S0642	4	IC, SDRAM, 4GBIT, DDR3-1600, C-DIE, 78P FBGA	U3000, U3010, U3020, U3030	CRITICAL	DRAM_TYPE=SAMSUNG_8GB
333S0642	4	IC, SDRAM, 4GBIT, DDR3-1600, C-DIE, 78P FBGA	U3100, U3110, U3120, U3130	CRITICAL	DRAM_TYPE=SAMSUNG_8GB
333S0642	4	IC, SDRAM, 4GBIT, DDR3-1600, C-DIE, 78P FBGA	U3200, U3210, U3220, U3230	CRITICAL	DRAM_TYPE=SAMSUNG_8GB
333S0628	4	IC, SDRAM, 2GBIT, DDR3L-1600, REV D, 78P FBGA	U2900, U2910, U2920, U2930	CRITICAL	DRAM_TYPE=ELPIDA_4GB
333S0628	4	IC, SDRAM, 2GBIT, DDR3L-1600, REV D, 78P FBGA	U3000, U3010, U3020, U3030	CRITICAL	DRAM_TYPE=ELPIDA_4GB
333S0628	4	IC, SDRAM, 2GBIT, DDR3L-1600, REV D, 78P FBGA	U3100, U3110, U3120, U3130	CRITICAL	DRAM_TYPE=ELPIDA_4GB
333S0628	4	IC, SDRAM, 2GBIT, DDR3L-1600, REV D, 78P FBGA	U3200, U3210, U3220, U3230	CRITICAL	DRAM_TYPE=ELPIDA_4GB
333S0629	4	IC, SDRAM, 4GBIT, DDR3L-1600, REV B, 78P FBGA	U2900, U2910, U2920, U2930	CRITICAL	DRAM_TYPE=ELPIDA_8GB
333S0629	4	IC, SDRAM, 4GBIT, DDR3L-1600, REV B, 78P FBGA	U3000, U3010, U3020, U3030	CRITICAL	DRAM_TYPE=ELPIDA_8GB
333S0629	4	IC, SDRAM, 4GBIT, DDR3L-1600, REV B, 78P FBGA	U3100, U3110, U3120, U3130	CRITICAL	DRAM_TYPE=ELPIDA_8GB
333S0629	4	IC, SDRAM, 4GBIT, DDR3L-1600, REV B, 78P FBGA	U3200, U3210, U3220, U3230	CRITICAL	DRAM_TYPE=ELPIDA_8GB

607-6811	1	ASSEMBLY, SUBASSY, DCBA, HALL EFFECT, K99	J6955	CRITICAL	
353S2929	1	IC, ISL6259, BATCHCHARGER, 3A, 4C400, QFN28	U7000	CRITICAL	
946-3116	1	MLB, DYNAX UV EB 0.22 GRAM, K78	GLUE	CRITICAL	

PD Module Parts

806-3706	1	CAN_TOPSIDE_COVER_ALT,J11/J13	TBTTOPSIDE_2P_COVER	CRITICAL	
806-3705	1	CAN_TOPSIDE_FENCE_ALT,J11/J13	TBTTOPSIDE_2P_FENCE	CRITICAL	
806-3214	1	CAN_TOPSIDE,J11/J13	TBTTOPSIDE_1P	CRITICAL	
806-3216	1	CAN_MDP,J11/J13	MDPCAN	CRITICAL	
806-3083	1	SHLD_USB_MLB,J11/J13	USBCAN	CRITICAL	
806-3142	1	CAN_TWT,J11/J13	TBTFENCE	CRITICAL	
806-3215	1	CAN_COVER_TBT,J11/J13	TBTCOVER	CRITICAL	

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BOM Configuration			
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Functional Test Points

J4001: AirPort / BT Connector

FUNC_TEST		
TRUE	PP3V3 WLAN F	(Need 6 TPs)
TRUE	WIFI EVENT L	
TRUE	PCIE AP R2D N	
TRUE	PCIE AP R2D P	
TRUE	PCIE CLK100M AP N	
TRUE	PCIE CLK100M AP P	
TRUE	USB BT CONN P	
TRUE	USB BT CONN N	
TRUE	PCIE AP D2R P	
TRUE	PCIE AP D2R N	
TRUE	PCIE WAKE L	
TRUE	AP RESET CONN L	
TRUE	AP CLKREQ O L	
TRUE	PP3V3 S3RS4 BT F	
(Need to add 8 GND TPs)		

J4501: SATA SSD Connector

FUNC_TEST		
TRUE	PP3V3 S0 SSD FLT	(Need 5 TPs)
TRUE	SATA SSD D2R P	
TRUE	SATA SSD D2R N	
TRUE	SATA SSD R2D N	
TRUE	SATA SSD R2D P	
TRUE	SMC QOBI RX L	
TRUE	SMC QOBI TX L	
TRUE	PCIE SSD D2R N<1>	
TRUE	PCIE SSD D2R P<1>	
TRUE	PCIE SSD R2D N<1>	
TRUE	PCIE SSD R2D P<1>	
TRUE	PCIE CLK100M SSD N	
TRUE	PCIE CLK100M SSD P	
TRUE	SSD CLKREQ L	
TRUE	SSD RESET L	
TRUE	SATA PCIE SEL	
TRUE	SSD P3V3S0 EN	
(Need to add 6 GND TPs)		

J4700: LIO Connector

FUNC_TEST		
TRUE	=PP3V42 G3H ONEMIRE	
TRUE	=PP3V3 S0 AUDIO	
TRUE	=PP3V3R1V5 S0 AUDIO	
TRUE	SYS ONEMIRE	
TRUE	SMC BC ACOK	
TRUE	=USB PWR EN	
TRUE	=I2C LIO SDA	
TRUE	=I2C LIO SCL	
TRUE	=I2C MIKEY SCL	
TRUE	=I2C MIKEY SDA	
TRUE	AUD IPHS SWITCH EN	
TRUE	AUD IP PERIPHERAL DET	
TRUE	AUD I2C INT L	
TRUE	AUD GPIO 3	
TRUE	SPKRAMP INR N	
TRUE	SPKRAMP INR P	
TRUE	USB EXT B N	
TRUE	USB EXT B P	
TRUE	USB CAMERA N	
TRUE	USB CAMERA P	
TRUE	HDA SDOUT	
TRUE	HDA BIT CLK	
TRUE	HDA SDINO	
TRUE	USB EXT B OC L	
TRUE	HDA RST L	
TRUE	HDA SYNC	
TRUE	USB3 EXT B RX RC N	
TRUE	USB3 EXT B RX RC P	
TRUE	USB3 EXT B TX C P	
TRUE	USB3 EXT B TX C N	
(Need to add 5 GND TPs)		

J5100: LPC+SPI Connector

FUNC_TEST		
TRUE	=PP3V3 S5 LPCPLUS	
TRUE	=PP5V S0 LPCPLUS	
TRUE	LPC AD<3..0>	
TRUE	SPI ALT MOSI	
TRUE	SPI ALT MISO	
TRUE	LPC FRAME L	
TRUE	PM CLKRUN L	
TRUE	SMC TMS	
TRUE	LPCPLUS RESET L	
TRUE	SMC TDO	
TRUE	TP SMC TRST L	
TRUE	TP SMC MD1	
TRUE	SMC TX L	
TRUE	LPC CLK33M LPCPLUS	
TRUE	SPIROM USE MLB	
TRUE	SPI ALT CLK	
TRUE	SPI ALT CS L	
TRUE	LPC SERIRQ	
TRUE	LPC PWRDWN L	
TRUE	SMC TDI	
TRUE	SMC TCK	
TRUE	SMC RESET L	
TRUE	SMC ROMBOOT	
TRUE	SMC RX L	
TRUE	LPCPLUS GPIO	
(Need to add 6 GND TPs)		

J5600: Fan Connector

FUNC_TEST		
TRUE	=PP5V S0 FAN	
TRUE	FAN RT TACH	
TRUE	FAN RT PWM	
(Need to add 1 GND TP)		

J5700: IPD Flex Connector

FUNC_TEST		
TRUE	SMC PME S4 WAKE L	
TRUE	PP5V TPAD FILT	
TRUE	=PP3V42 G3H TPAD	
TRUE	PP3V3 TPAD CONN	
TRUE	USB TPAD P	
TRUE	USB TPAD N	
TRUE	=I2C TPAD SDA	
TRUE	=I2C TPAD SCL	
TRUE	SMC ONOFF L	
TRUE	SMC LID	
TRUE	SMC TPAD RST L	
(Need to add 5 GND TPs)		

J6900: DC-In Connector

FUNC_TEST		
TRUE	=PP18V5 DCIN CONN	
TRUE	=PP5V S3 LIO CONN	
(Need to add 5 GND TPs)		

J6903: Speaker Connector

FUNC_TEST		
TRUE	SPKRAMP ROUT P	
TRUE	SPKRAMP ROUT N	
(Need to add 3 GND TPs)		

J6950: Battery Connector

FUNC_TEST		
TRUE	PPVBAT G3H CONN	
TRUE	=SMBUS BATT SCL	
TRUE	=SMBUS BATT SDA	
TRUE	SYS DETECT L	
(Need to add 4 GND TPs near J6950 and 1 for shield)		

J9000: Internal DP Connector

FUNC_TEST		
TRUE	PPVOUT SW LCDBKLT	
TRUE	PP3V3 SW LCD	
TRUE	I2C TCON SDA R	
TRUE	LED RETURN 6	
TRUE	LED RETURN 5	
TRUE	LED RETURN 4	
TRUE	LED RETURN 3	
TRUE	LED RETURN 2	
TRUE	LED RETURN 1	
TRUE	DP INT HPD CONN	
TRUE	DP INT AUX CH C N	
TRUE	DP INT AUX CH C P	
TRUE	DP INT ML F P<0>	
TRUE	DP INT ML F N<0>	
TRUE	I2C TCON SCL R	
(Need to add 5 GND TPs)		

J5715: KB BKLT Connector

FUNC_TEST		
TRUE	KBDLED FB	
TRUE	KBDLED ANODE	
(Need to add 2 GND TPs)		

J6955: HALL EFFECT Connector

FUNC_TEST		
TRUE	SMC LID R	
TRUE	=PP3V42 G3H HALL	

Misc Voltages & Control Signals

FUNC_TEST		
TRUE	PPBUS G3H	
TRUE	PPVIN SW TBTBST	
TRUE	PPBUS S5 HS COMPUTING ISNS	
TRUE	PPDCIN G3H	
TRUE	PP3V42 G3H	
TRUE	PPVRTC G3H	
TRUE	PP5V S5	
TRUE	PP5V SUS	
TRUE	PP3V3 S5	
TRUE	PP3V3 SUS	
TRUE	PP3V3 S3	
TRUE	PP1V8 S0	
TRUE	PP3V3 S0	
TRUE	PP1V5 S3	
TRUE	PP1V5 S3RS0	
TRUE	PP1V5 S0	
TRUE	PP1V05 S0	
TRUE	PPVTTDDR S3	
TRUE	PP0V75 S0 DDRVTT	
TRUE	PPVCCSA S0 CPU	
TRUE	PP1V05 SUS	
TRUE	PP15V TBT	
TRUE	PP3V3 TBTLC	
TRUE	PP1V05 TBTLC	
TRUE	PP1V05 S0 PCH VCCADPLL	
TRUE	PPVCORE S0 CPU	
TRUE	PPVCORE S0 AXG	
TRUE	PP1V5 S3 CPU VCCDQ	
TRUE	PP1V05 S0 CPU VCCPQ	
TRUE	PP1V8 S0 CPU VCCPLL R	
TRUE	PP1V05 TBTIC0	
TRUE	PPBUS S5 HS OTHER ISNS	
TRUE	PPDCIN G3H ISOL	
TRUE	PP5V S3	
TRUE	PP5V S0	
TRUE	PP3V3 S4	

NO_TEST Nets

POWER SIGNALS		
NO_TEST		
TP CRT IG BLUE	TRUE	NC CRT IG BLUE
TP CRT IG GREEN	TRUE	NC CRT IG GREEN
TP CRT IG RED	TRUE	NC CRT IG RED
TP CRT IG DDC CLK	TRUE	NC CRT IG DDC CLK
TP CRT IG DDC DATA	TRUE	NC CRT IG DDC DATA
TP CRT IG HSYNC	TRUE	NC CRT IG HSYNC
TP CRT IG VSYNC	TRUE	NC CRT IG VSYNC
TP LVDS IG CTRL CLK	TRUE	NC LVDS IG CTRL CLK
TP LVDS IG CTRL DATA	TRUE	NC LVDS IG CTRL DATA
TP PCH LVDS VBI	TRUE	NC PCH LVDS VBI
TP HDA SDIN1	TRUE	NC HDA SDIN1
TP HDA SDIN2	TRUE	NC HDA SDIN2
TP HDA SDIN3	TRUE	NC HDA SDIN3
TP PCI PME L	TRUE	NC PCI PME L
TP PCI CLK33M OUT3	TRUE	NC PCI CLK33M OUT3
TP CLINK CLK	TRUE	NC CLINK CLK
TP CLINK DATA	TRUE	NC CLINK DATA
TP CLINK RESET L	TRUE	NC CLINK RESET L
TP PCIE CLK100M PERN	TRUE	NC PCIE CLK100M PERN
TP PCIE CLK100M PERP	TRUE	NC PCIE CLK100M PERP
TP SDVO TVCLKINH	TRUE	NC SDVO TVCLKINH
TP SDVO TVCLKINP	TRUE	NC SDVO TVCLKINP
TP SDVO STALLN	TRUE	NC SDVO STALLN
TP SDVO STALLP	TRUE	NC SDVO STALLP
TP SDVO INTN	TRUE	NC SDVO INTN
TP SDVO INTP	TRUE	NC SDVO INTP
TP XDP PCH OBSFN A<0..1>	TRUE	NC TP XDP PCH OBSFN A<0..1>
TP XDP PCH OBSFN B<0..1>	TRUE	NC TP XDP PCH OBSFN B<0..1>
TP XDPPCH HOOK2	TRUE	NC TP XDPPCH HOOK2
TP XDPPCH HOOK3	TRUE	NC TP XDPPCH HOOK3
TP XDP PCH OBSFN D<0..1>	TRUE	NC TP XDP PCH OBSFN D<0..1>
TP XDP PCH HOOK4	TRUE	NC TP XDP PCH HOOK4
TP XDP PCH HOOK5	TRUE	NC TP XDP PCH HOOK5
TP PCH GPIO64 CLKOUTFLX0	TRUE	NC PCH GPIO64 CLKOUTFLX0
TP PCH GPIO65 CLKOUTFLX1	TRUE	NC PCH GPIO65 CLKOUTFLX1
TP PCH GPIO66 CLKOUTFLX2	TRUE	NC PCH GPIO66 CLKOUTFLX2
TP PCH GPIO67 CLKOUTFLX3	TRUE	NC PCH GPIO67 CLKOUTFLX3

NC EDP TXP<0..3>	TRUE	TP EDP TX P<0..3>
MAKE_BASE=TRUE		
NC EDP TXN<0..3>	TRUE	TP EDP TX N<0..3>
MAKE_BASE=TRUE		
NC EDP AUXN	TRUE	TP EDP AUX P
MAKE_BASE=TRUE		
NC EDP AUXN	TRUE	TP EDP AUX N
MAKE_BASE=TRUE		
NC CPU THERMDA	TRUE	TP CPU THERMDA
MAKE_BASE=TRUE		
NC CPU THERMDC	TRUE	TP CPU THERMDC
MAKE_BASE=TRUE		
NC CPU RSVD<30..45>	TRUE	TP CPU RSVD<30..45>
MAKE_BASE=TRUE		
NC CPU RSVD<8..27>	TRUE	TP CPU RSVD<8..27>
MAKE_BASE=TRUE		


NC PEG R2D CP<15..2>	TRUE	=PEG R2D C P<15..2>
MAKE_BASE=TRUE		
NC PEG R2D CN<15..2>	TRUE	=PEG R2D C N<15..2>
MAKE_BASE=TRUE		
NC PEG D2RP<15..2>	TRUE	=PEG D2R P<15..2>
MAKE_BASE=TRUE		
NC PEG D2RN<15..2>	TRUE	=PEG D2R N<15..2>
MAKE_BASE=TRUE		

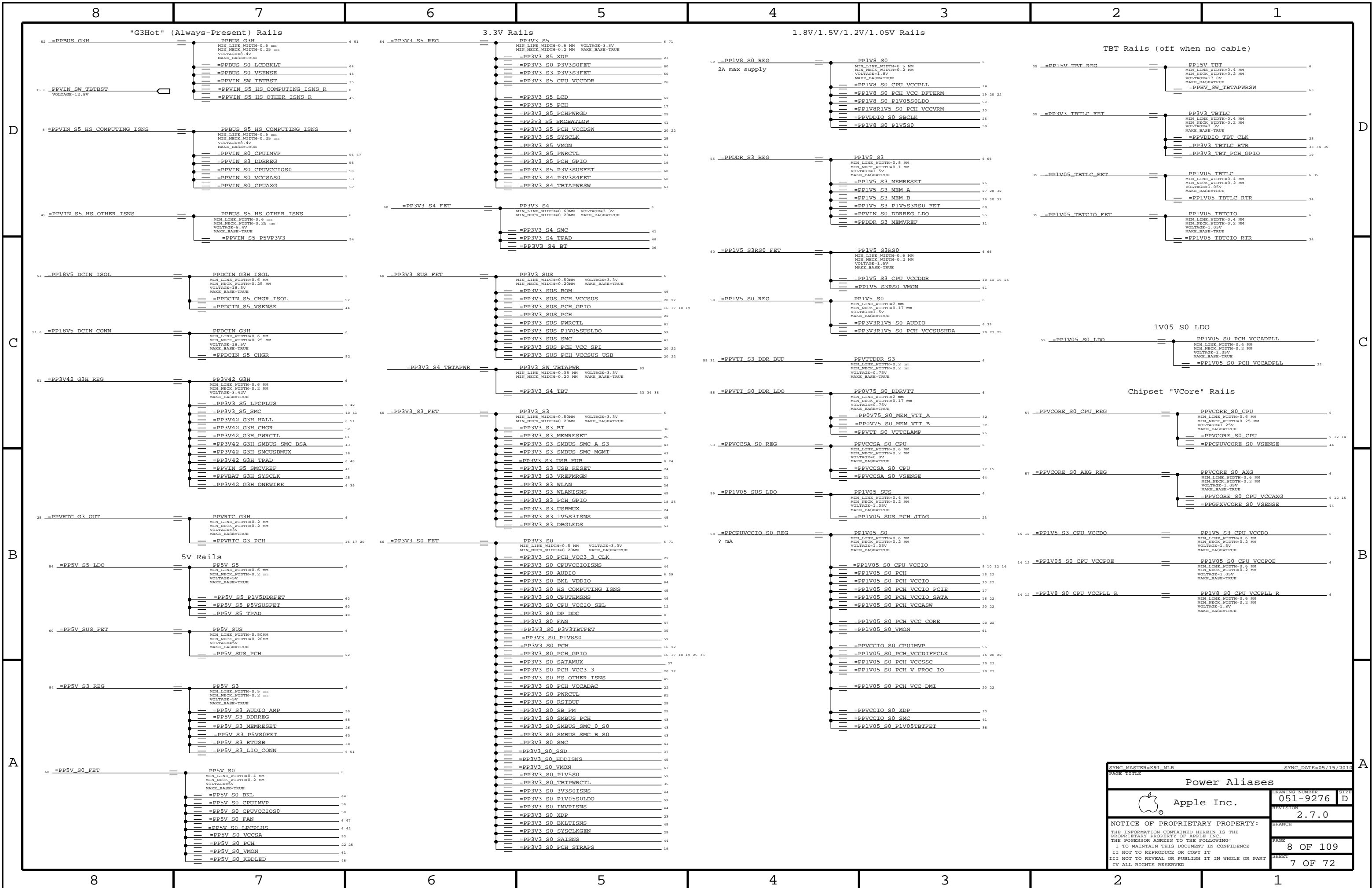
TP PCIE CLK100M PE4N	TRUE	NC PCIE CLK100M PE4N
TP PCIE CLK100M PE4P	TRUE	NC PCIE CLK100M PE4P
TP PCIE CLK100M PE5N	TRUE	NC PCIE CLK100M PE5N
TP PCIE CLK100M PE5P	TRUE	NC PCIE CLK100M PE5P
TP PCIE CLK100M PE6N	TRUE	NC PCIE CLK100M PE6N
TP PCIE CLK100M PE6P	TRUE	NC PCIE CLK100M PE6P
TP PCIE CLK100M PE7N	TRUE	NC PCIE CLK100M PE7N
TP PCIE CLK100M PE7P	TRUE	NC PCIE CLK100M PE7P
TP PSOC P1 3	TRUE	NC PSOC P1 3
TP SATA B D2RN	TRUE	NC SATA B D2RN
TP SATA B D2RP	TRUE	NC SATA B D2RP
TP SATA B R2D CN	TRUE	NC SATA B R2D CN
TP SATA B R2D CP	TRUE	NC SATA B R2D CP
TP SATA D D2RN	TRUE	NC SATA D D2RN
TP SATA D D2RP	TRUE	NC SATA D D2RP
TP SATA D R2D CN	TRUE	NC SATA D R2D CN
TP SATA D R2D CP	TRUE	NC SATA D R2D CP
TP SATA E D2RN	TRUE	NC SATA E D2RN
TP SATA E D2RP	TRUE	NC SATA E D2RP
TP SATA E R2D CN	TRUE	NC SATA E R2D CN
TP SATA E R2D CP	TRUE	NC SATA E R2D CP
TP SATA F D2RN	TRUE	NC SATA F D2RN
TP SATA F D2RP	TRUE	NC SATA F D2RP
TP SATA F R2D CN	TRUE	NC SATA F R2D CN
TP SATA F R2D CP	TRUE	NC SATA F R2D CP

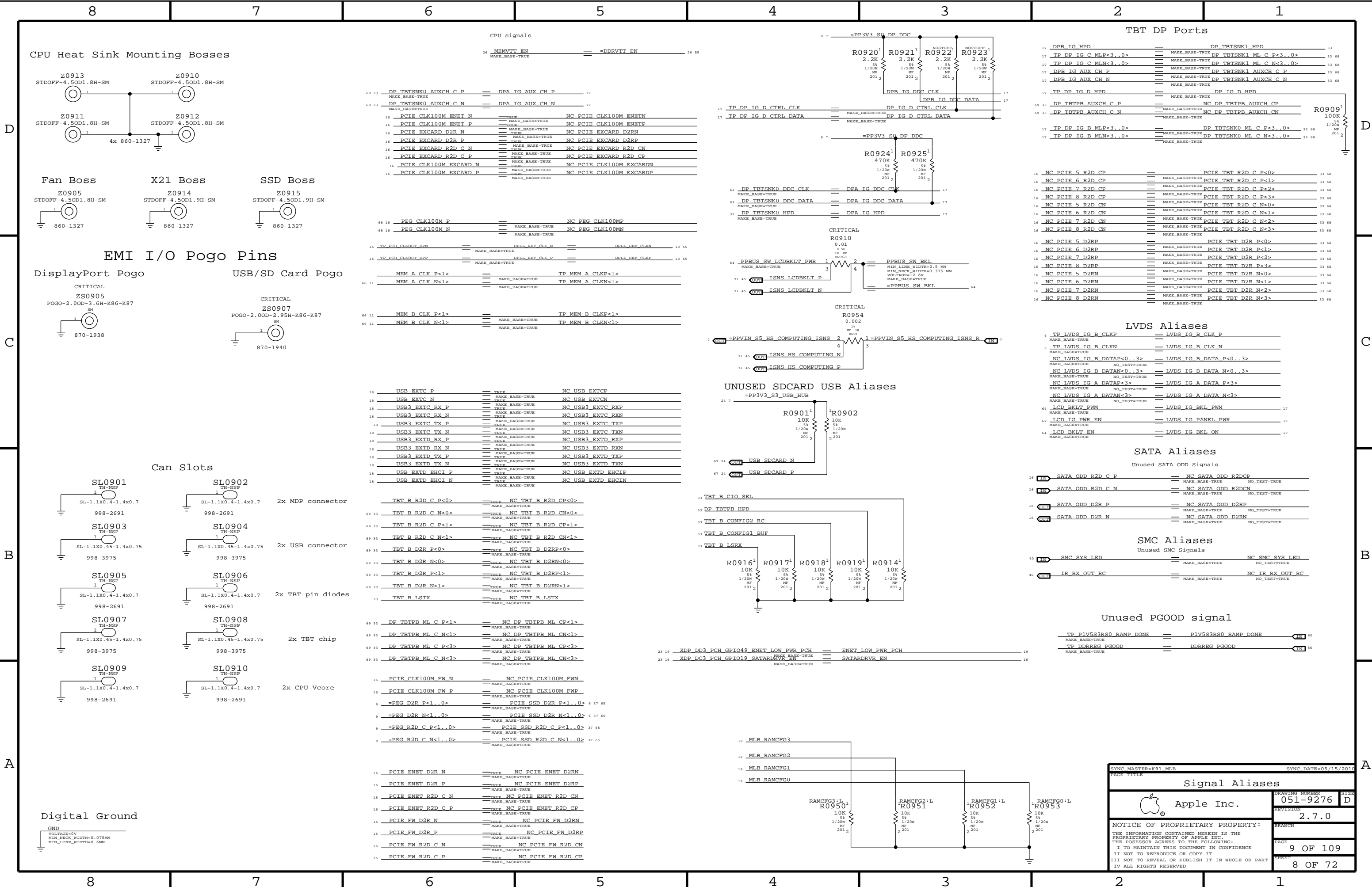
TP PCH TP18	TRUE	NC PCH TP18
TP PCH TP17	TRUE	NC PCH TP17
TP PCH TP16	TRUE	NC PCH TP16
TP PCH TP15	TRUE	NC PCH TP15
TP PCH TP14	TRUE	NC PCH TP14
TP PCH TP13	TRUE	NC PCH TP13
TP PCH TP12	TRUE	NC PCH TP12
TP PCH TP10	TRUE	NC PCH TP10
TP PCH TP9	TRUE	NC PCH TP9
TP PCH TP8	TRUE	NC PCH TP8
TP PCH TP7	TRUE	NC PCH TP7
TP PCH TP6	TRUE	NC PCH TP6
TP PCH TP5	TRUE	NC PCH TP5
TP PCH TP4	TRUE	NC PCH TP4
TP PCH TP3	TRUE	NC PCH TP3
TP PCH TP2	TRUE	NC PCH TP2
TP PCH TP1	TRUE	NC PCH TP1

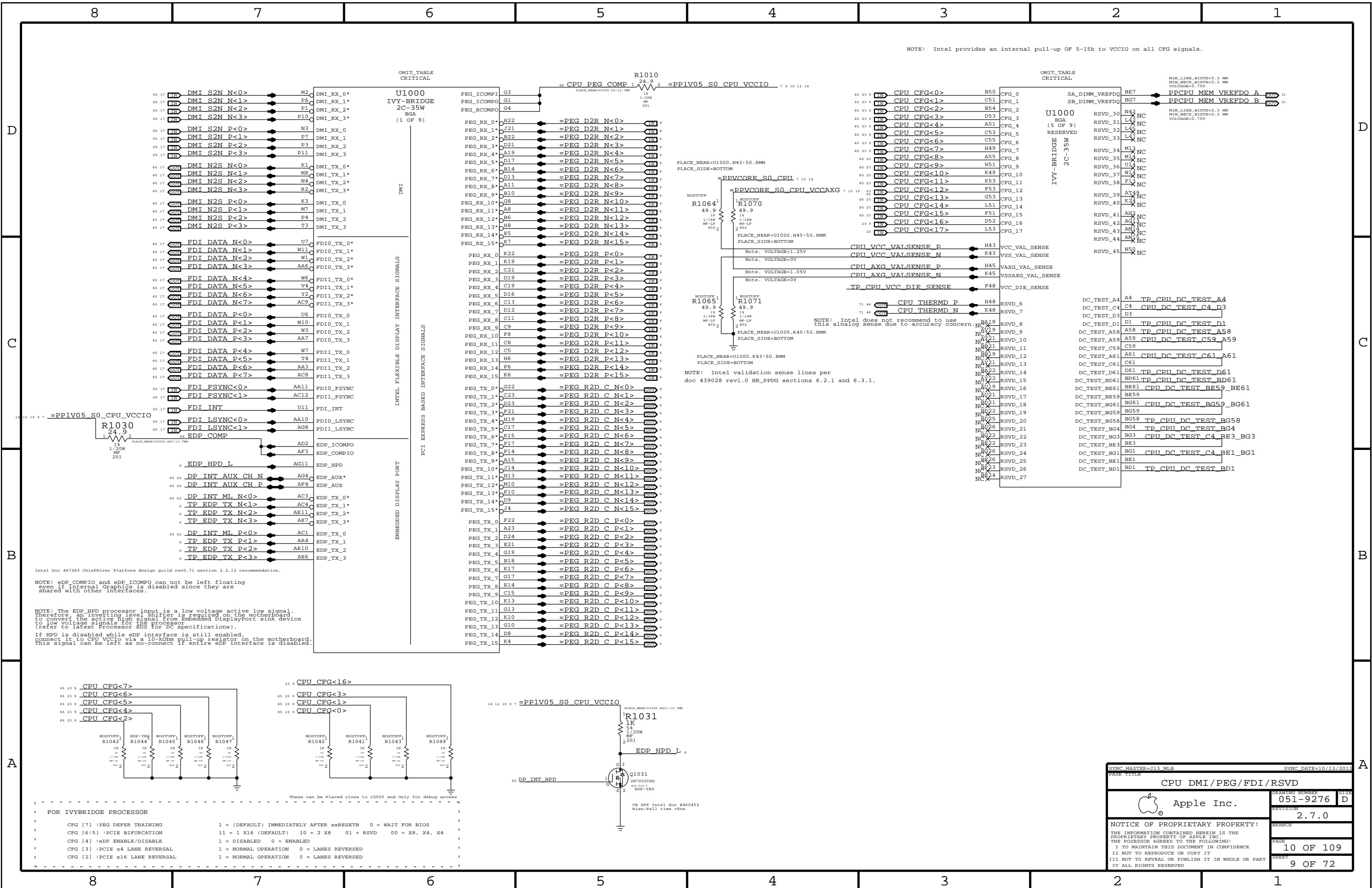
TP LVDS IG B CLKN	TRUE	NC LVDS IG B CLKN
TP LVDS IG B CLKP	TRUE	NC LVDS IG B CLKP
TP LVDS IG BK1 PWM	TRUE	NC LVDS IG BK1 PWM

SMC BS ALRT L	TRUE	NC SMC BS ALRT L
---------------	------	------------------

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D

C

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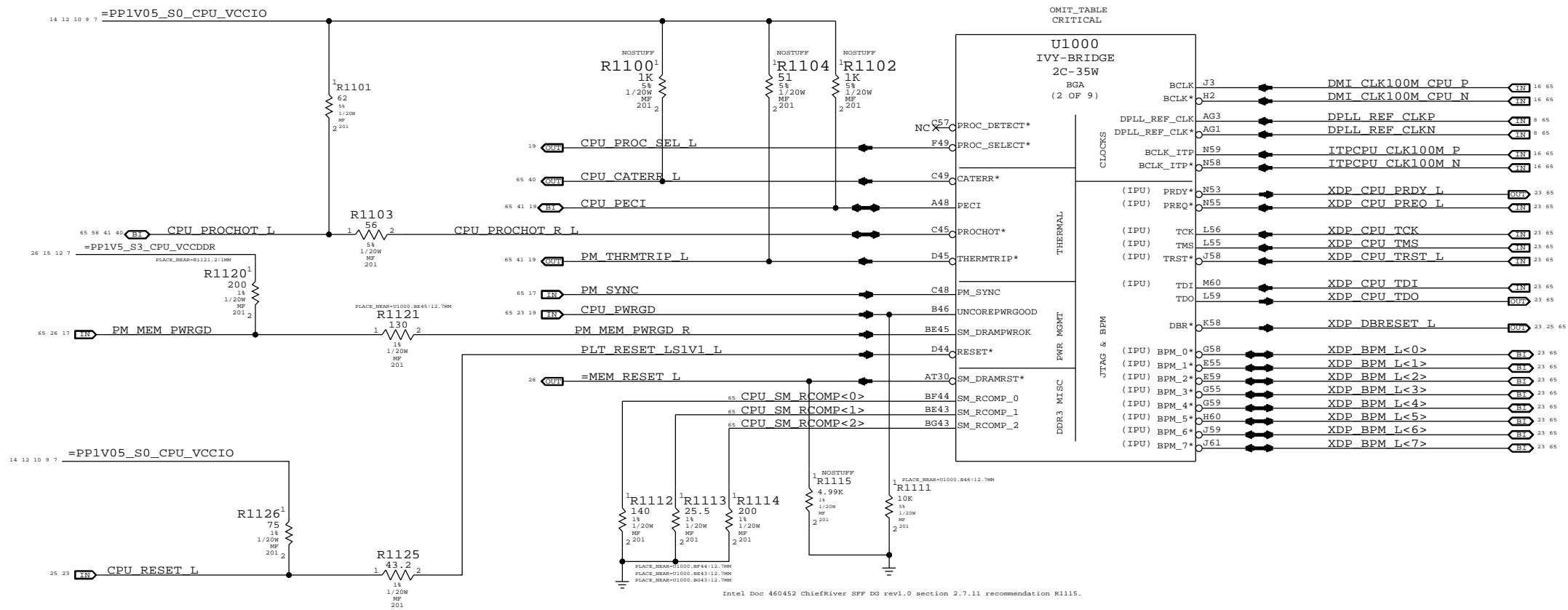
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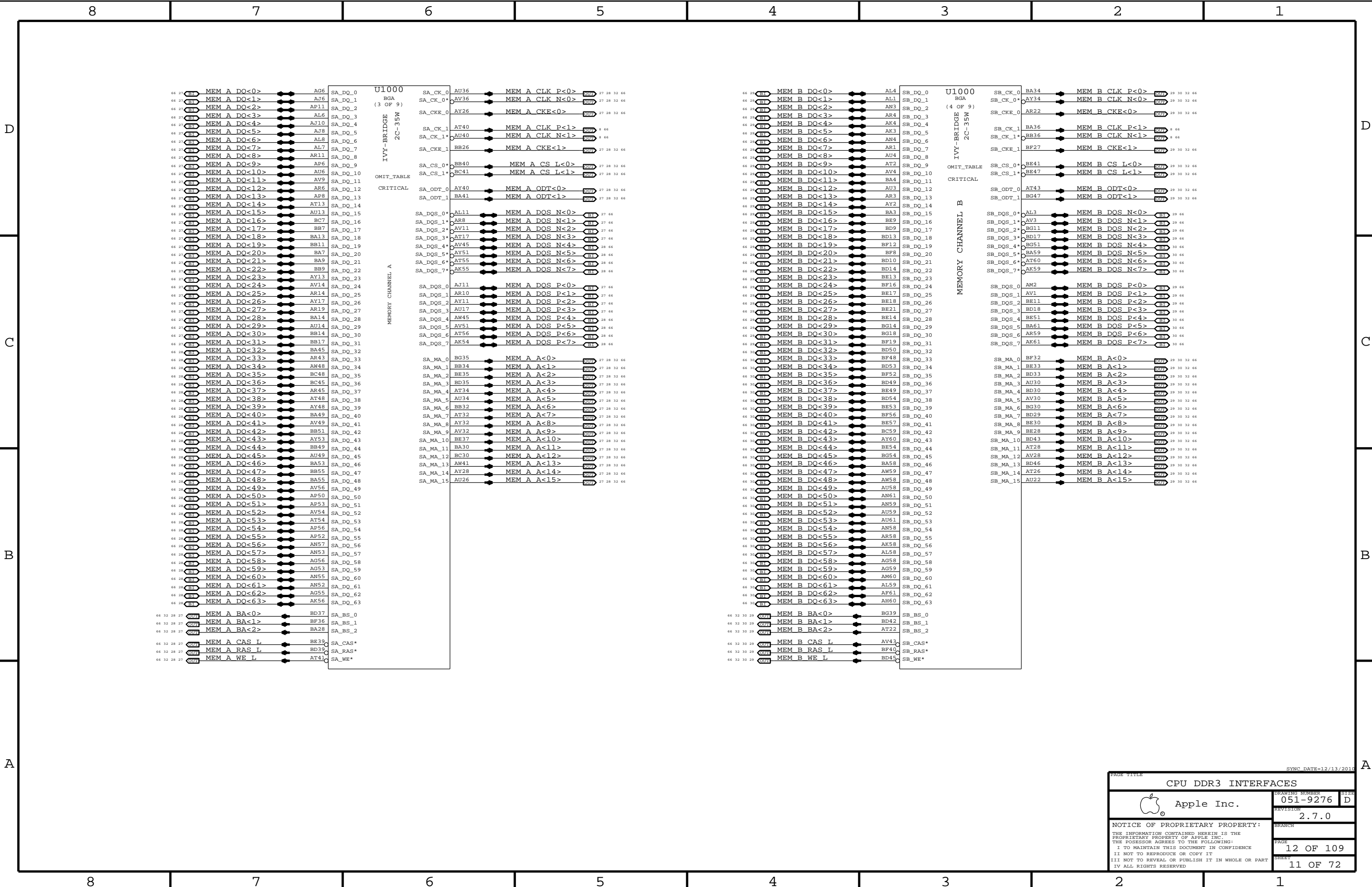
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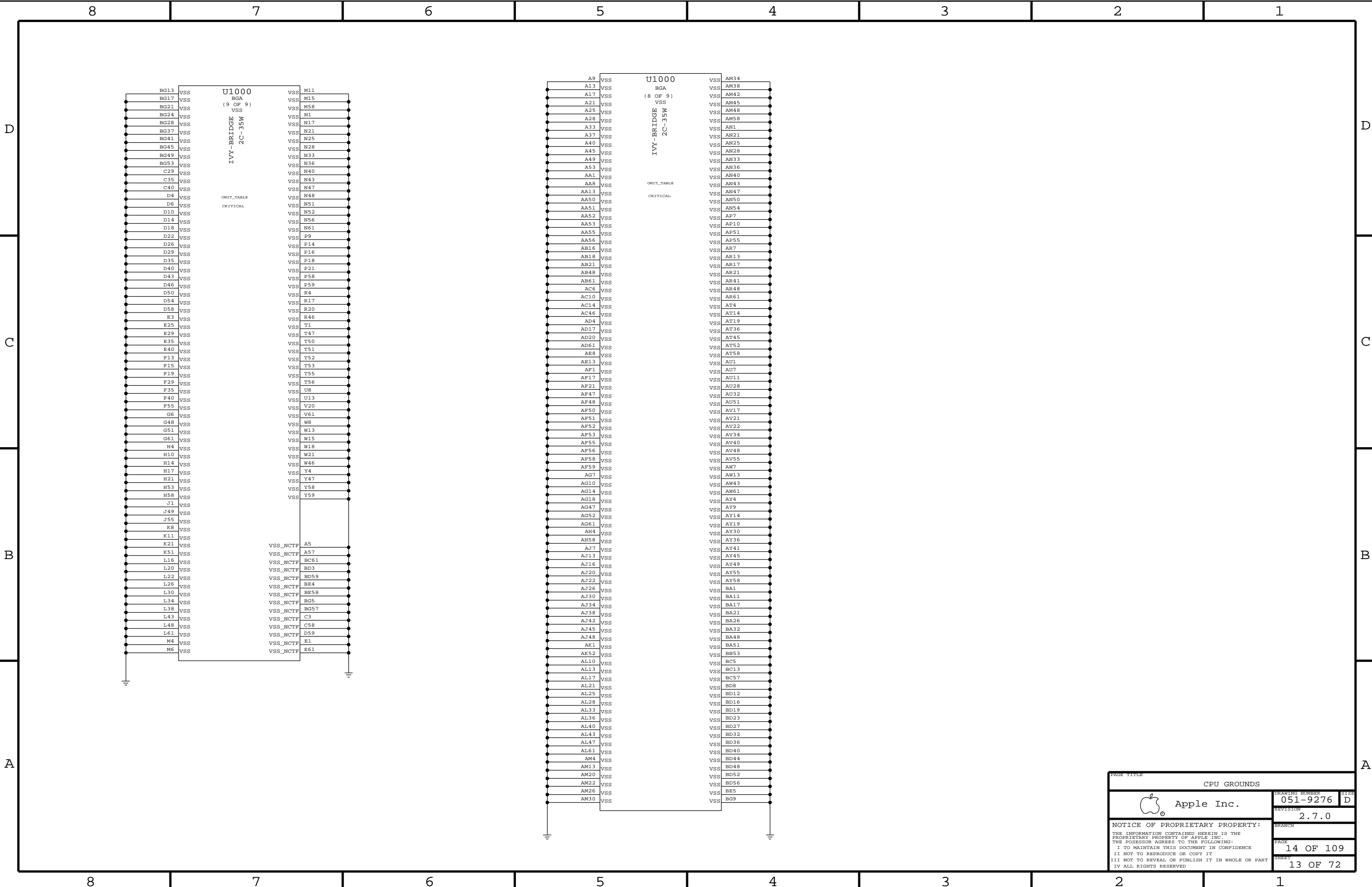
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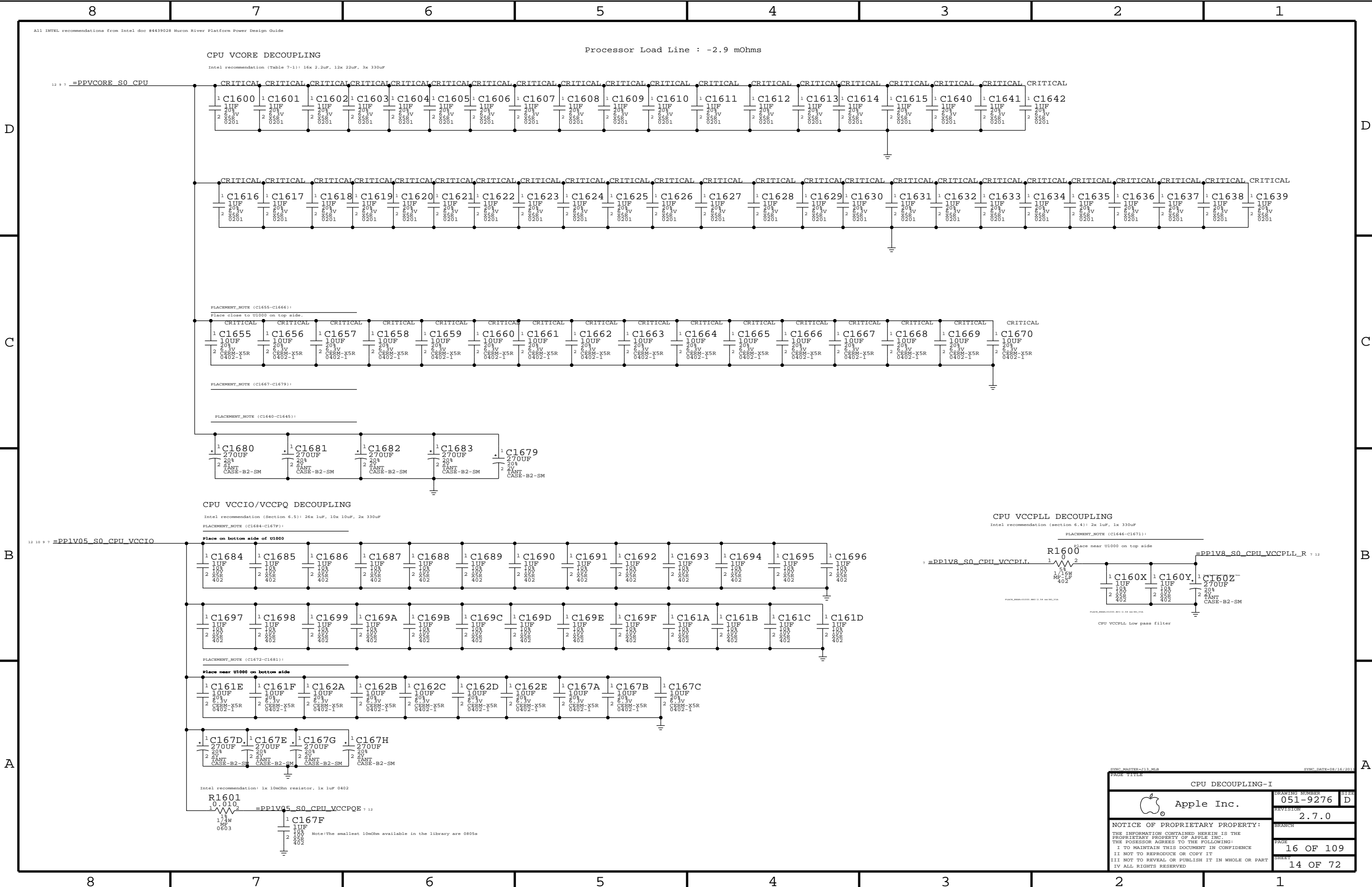


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CPU CLOCK/MISC/JTAG			
 Apple Inc.	DRAWING NUMBER	051-9276	SIZE D
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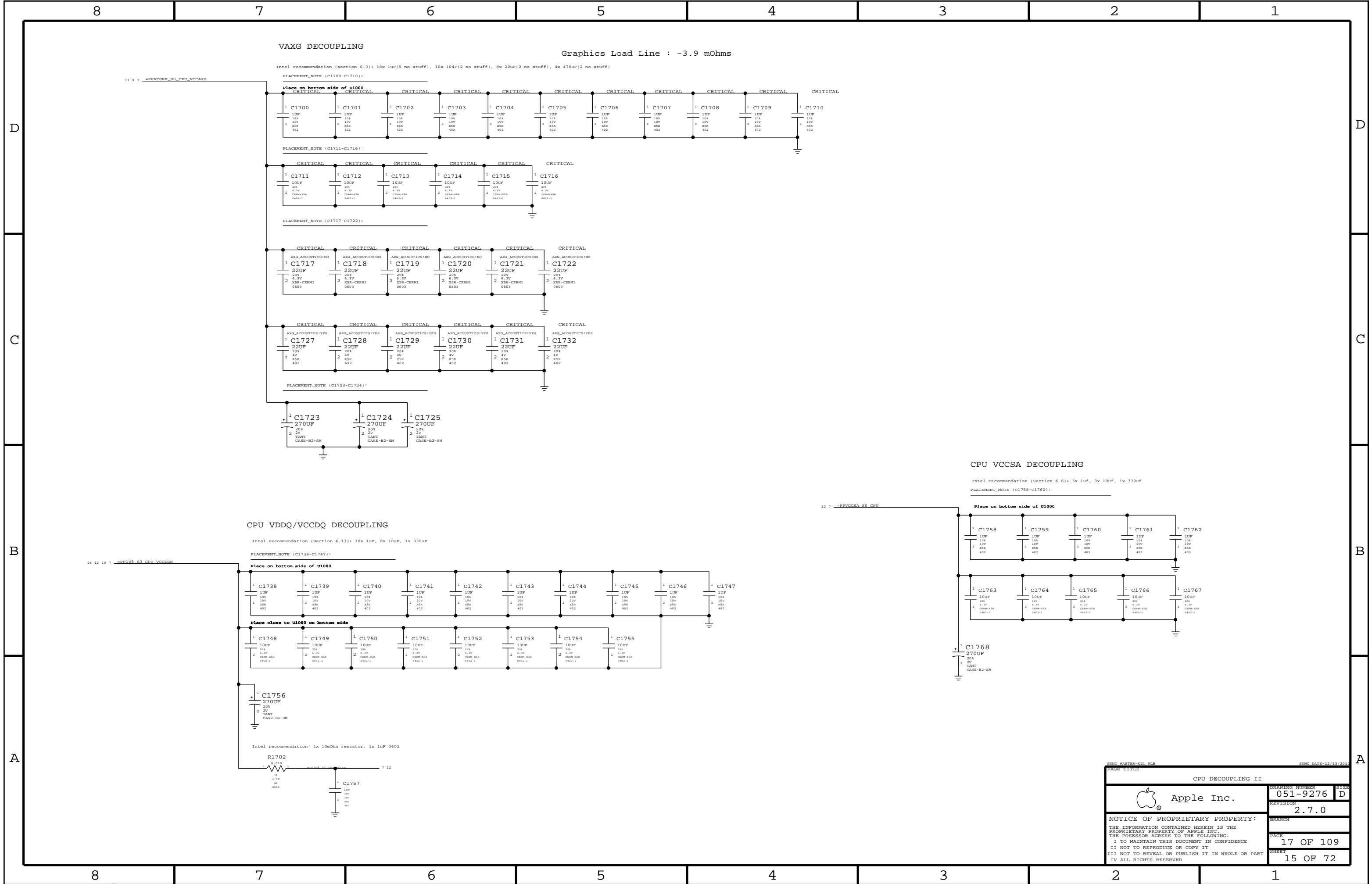








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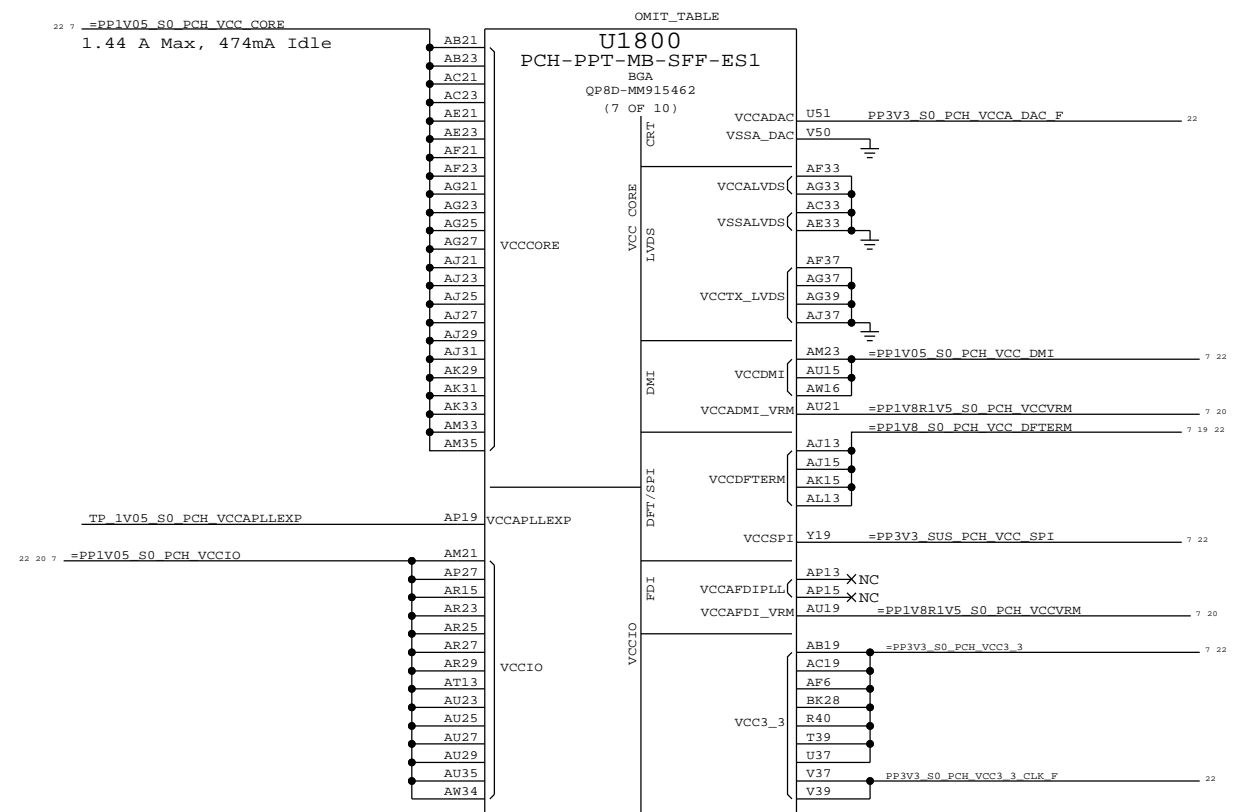
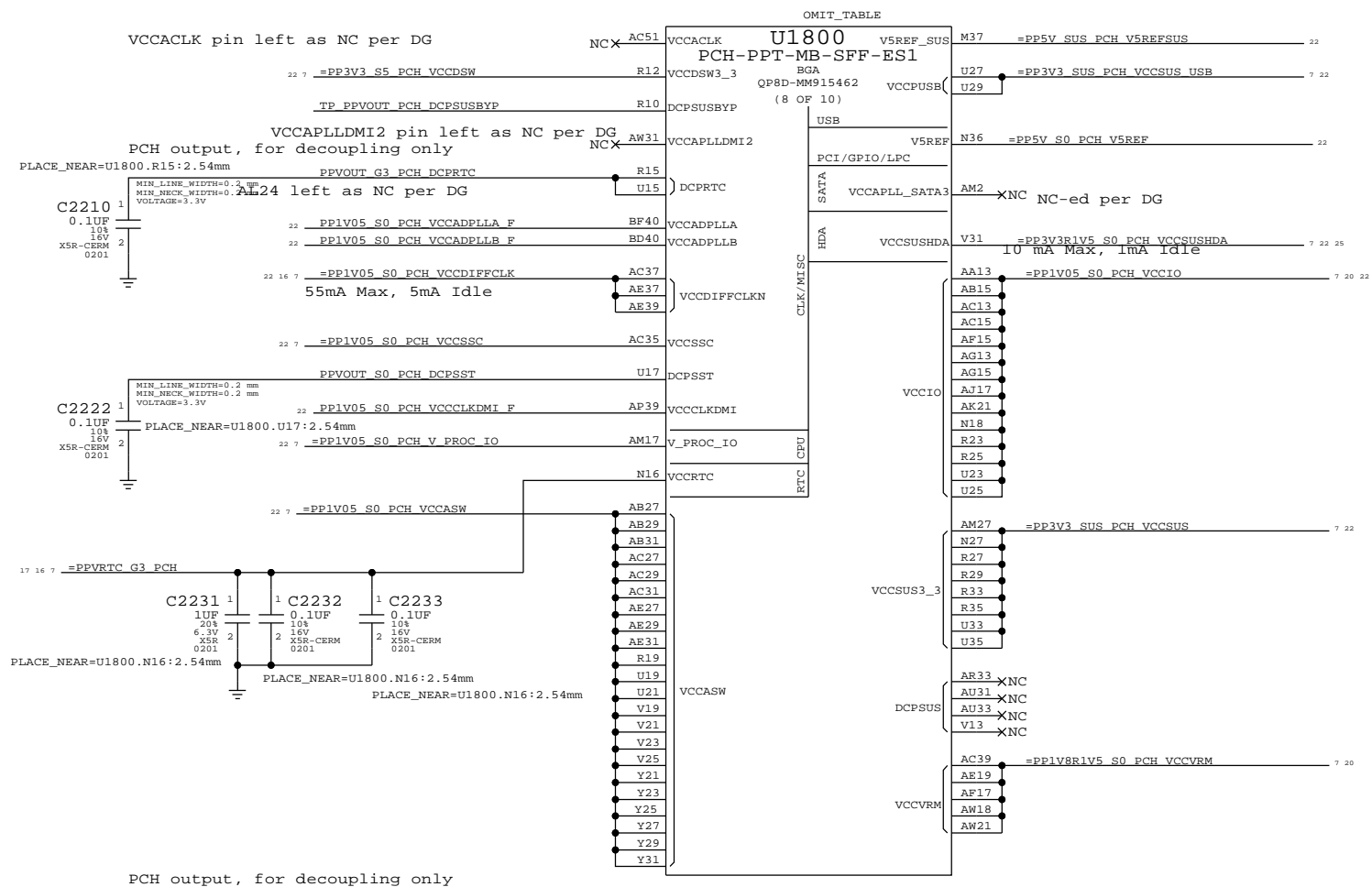


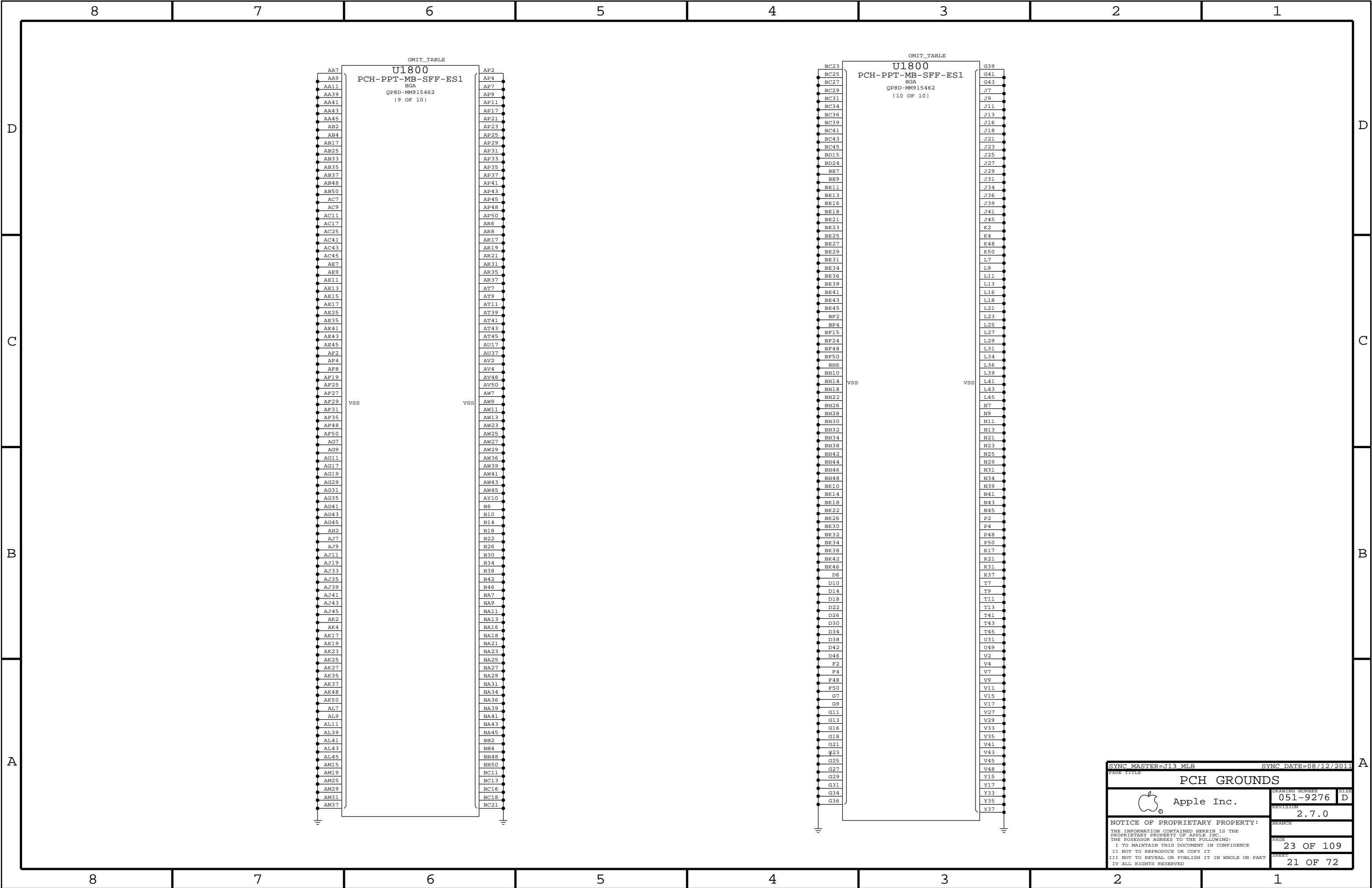













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SYNC DATE=08/12/2011

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PCH GROUNDS

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051-9276

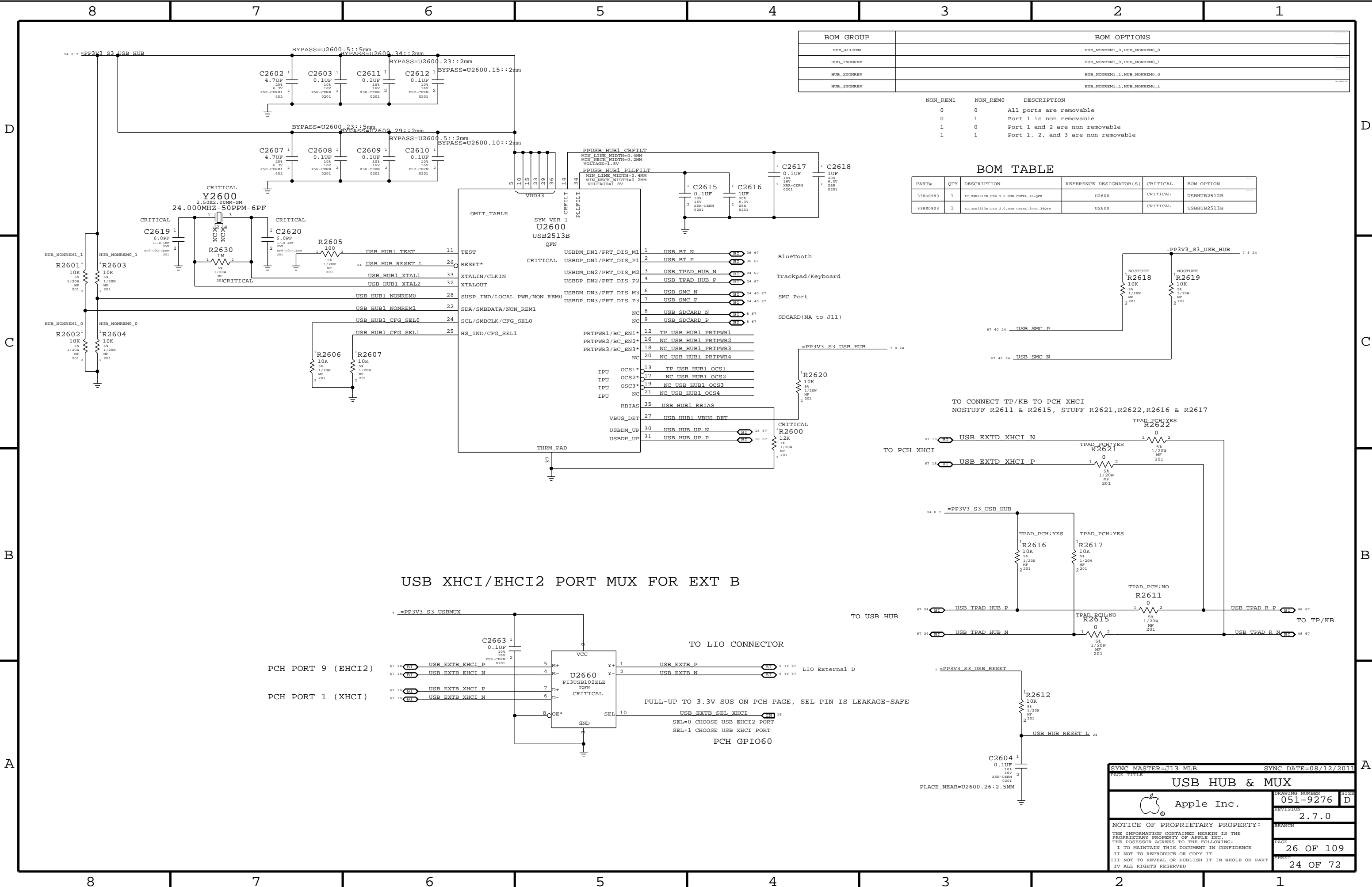
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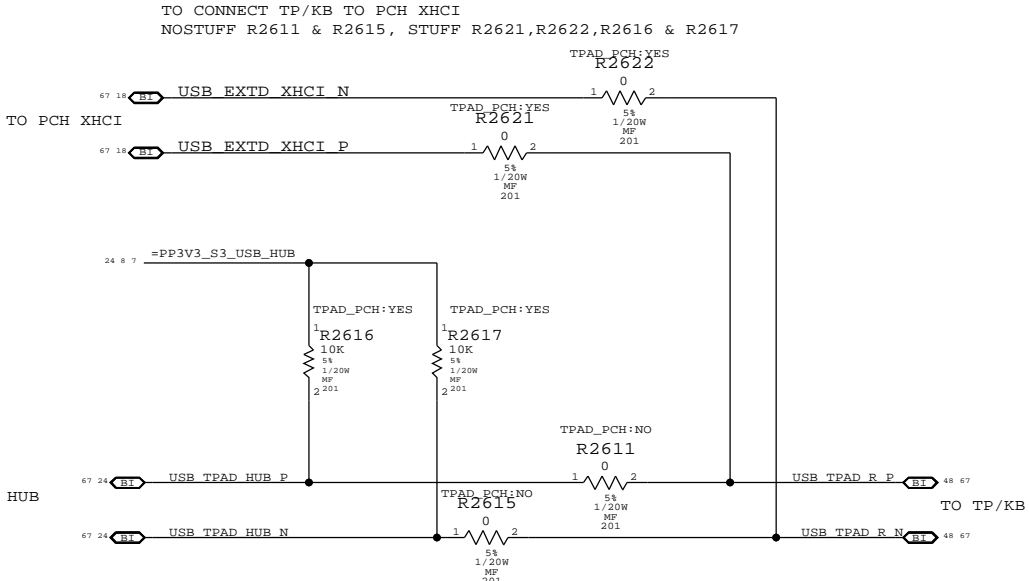
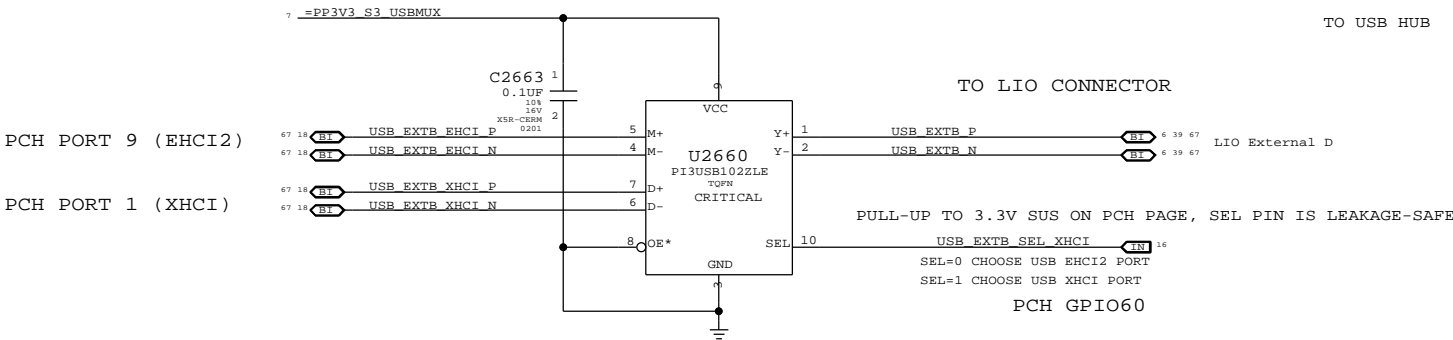


BOM GROUP	BOM OPTIONS
HUB_ALLREM	HUB_NONREM1_0,HUB_NONREM0_0
HUB_1NONREM	HUB_NONREM1_0,HUB_NONREM0_1
HUB_2NONREM	HUB_NONREM1_1,HUB_NONREM0_0
HUB_3NONREM	HUB_NONREM1_1,HUB_NONREM0_1

NON_REM1	NON_REM0	DESCRIPTION
0	0	All ports are removable
0	1	Port 1 is non removable
1	0	Port 1 and 2 are non removable
1	1	Port 1, 2, and 3 are non removable

BOM TABLE					
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
33880983	1	IC,USB2512B,USB 2.0 HUB CTRL,36-QFN	U2600	CRITICAL	USBHUB2512B
33880923	1	IC,USB2513B,USB 2.0 HUB CTRL,SPRT,36QFN	U2600	CRITICAL	USBHUB2513B

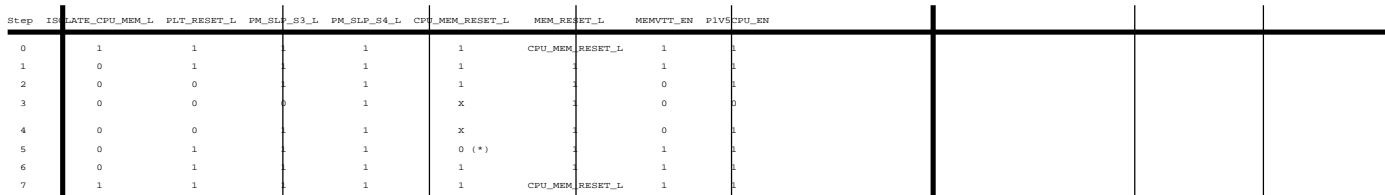
USB XHCI/EHCI2 PORT MUX FOR EXT B



PAGE TITLE		PAGE TITLE	
USB HUB & MUX		USB HUB & MUX	
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WHEN LOW: CPU 1.5V follows S0 rails, VTT ensures clean CKE transition, MEM_RESET_L isolated.

```
MEM_RESET_L = !ISOLATE_CPU_MEM_L + CPU_MEM_RESET_L
```




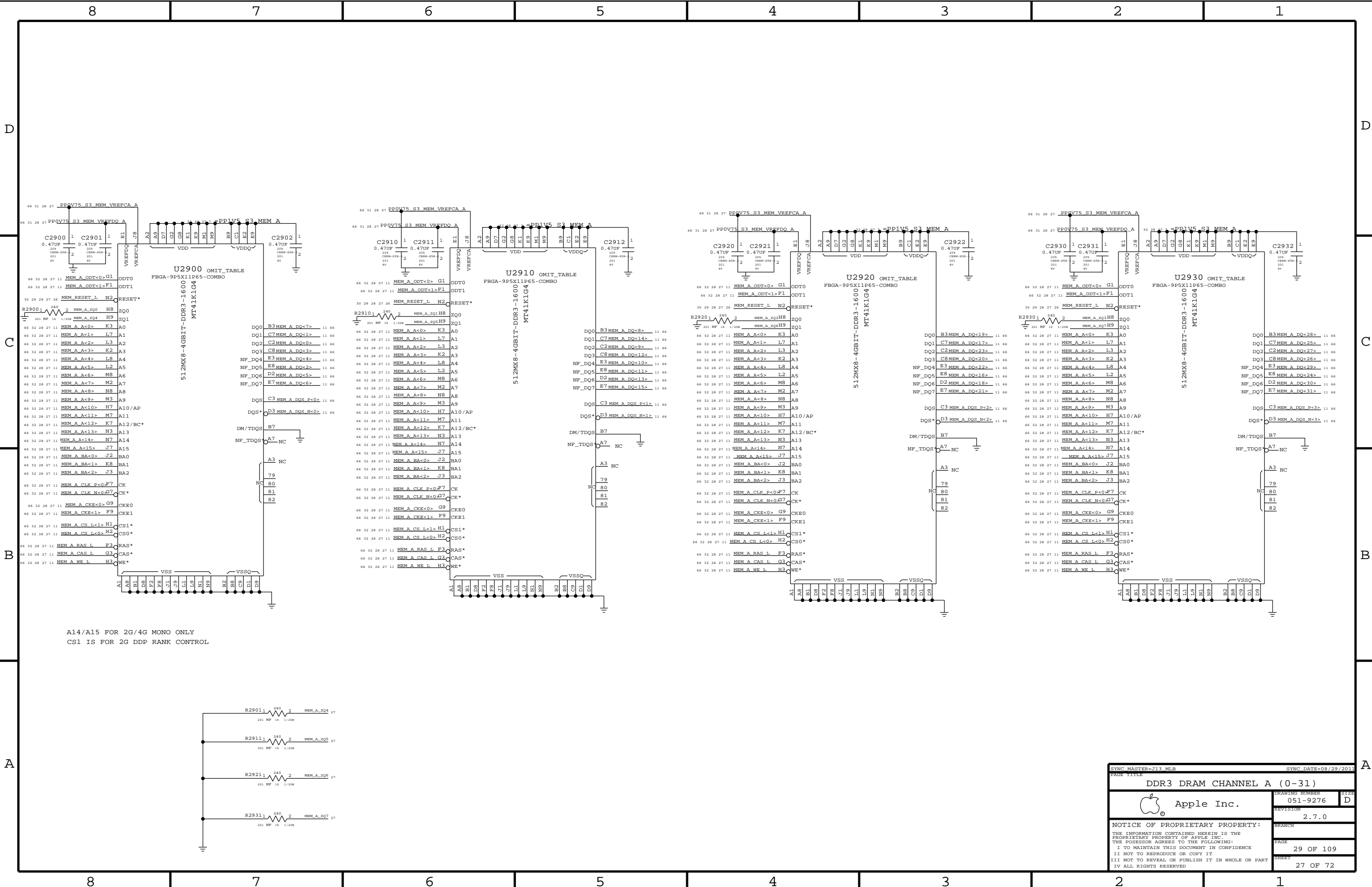
NOTE: In the event of a S3->S5 transition ISOLATE_CPU_MEM_L will still be asserted on next S5->S0 transition. Rails will power-up as if from S3, but MEM_RESET_L will not properly assert. Software must deassert ISOLATE_CPU_MEM_L and then generate a valid reset cycle on CPU_MEM_RESET_L.

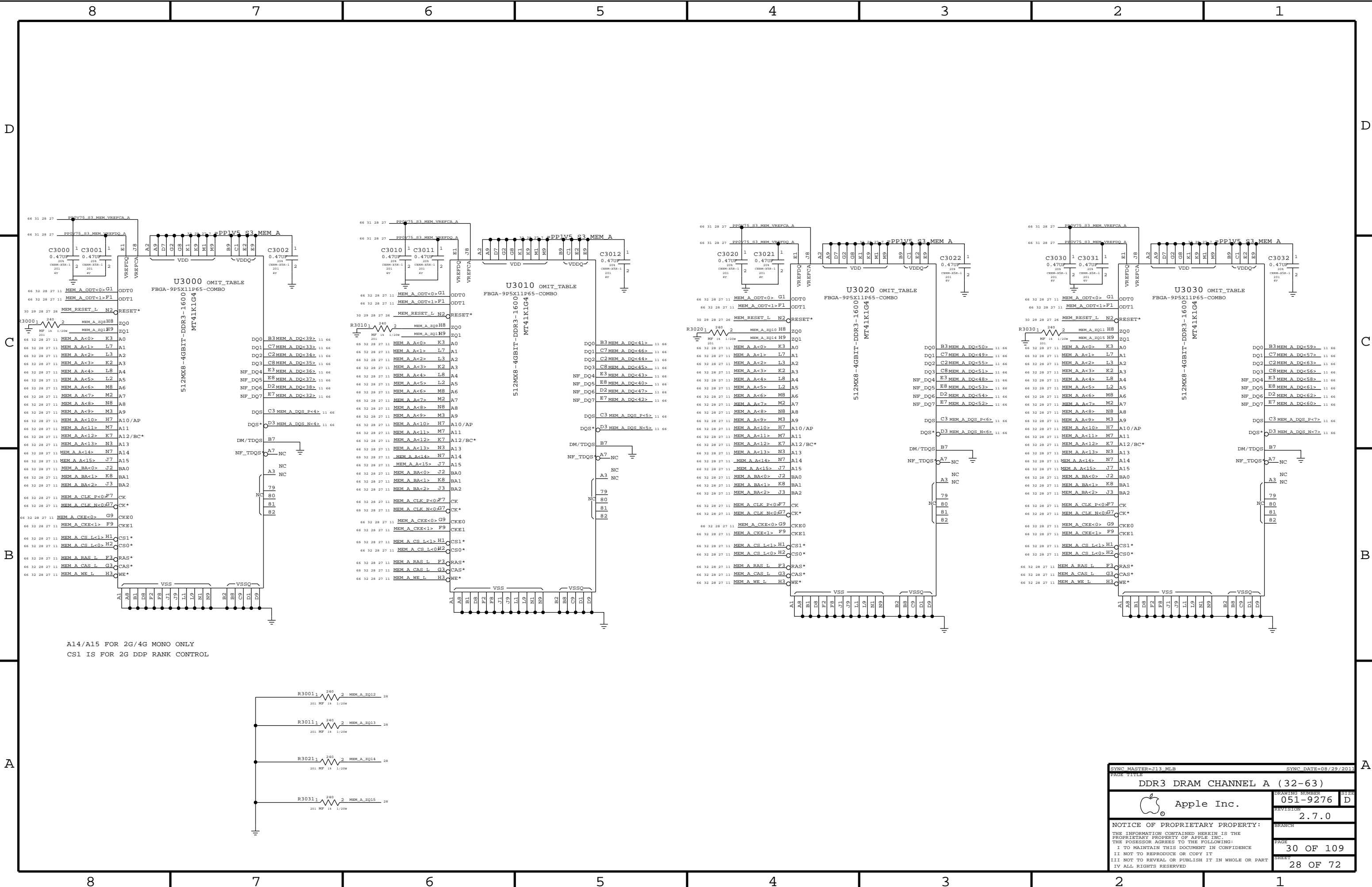
The schematic diagram illustrates the VTTCLAMP circuit. It features two NPN transistors, Q2850 (SSM6N37FEAPE SOT563), configured as emitter followers. The base of the first transistor (top) is connected to the VTTCLAMP_EN signal through a 100K resistor (R2851). Its emitter is connected to the VTTCLAMP_L node, which also receives current from a 75mA max load @ 0.75V supply (R2850) and provides 60mW max power. A 100nF capacitor (C2851) is connected between the collector and emitter of the top transistor. The base of the second transistor (bottom) is connected to the VTTCLAMP_EN signal through a 100K resistor (R2851). Its emitter is connected to ground. A 100nF capacitor (C2851) is connected between the collector and emitter of the bottom transistor. The VTTCLAMP_L node is connected to the collector of the top transistor and the collector of the bottom transistor.

	Step	IS_DATE_CPU_MEM_L	PLT_RESET_L	PM_SLP_S3_L	PM_SLP_S4_L	CPU_MEM_RESET_L	MEM_RESET_L	MEMVTT_KN	PIVE	CPU_KN			
S0	0	1	1	1	1	1	CPU_MEM_RESET_L	1	1	1			
	1	0	1	1	1	1		1	1	1			
to	2	0	0	1	1	1		0	1	1			
	3	0	0	0	1	X	1	0	0	0			
S3	4	0	0	1	1	X	1	0	1	1			
	5	0	1	1	1	0 (*)	1	1	1	1			
to	6	0	1	1	1	1	1	1	1	1			
S0	7	1	1	1	1	1	CPU_MEM_RESET_L	1	1	1			

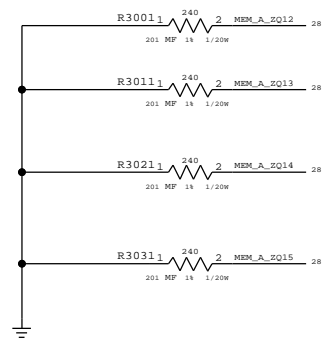
NOTE: In the event of a S3->S5 transition ISOLATE_CPU_MEM_L will still be asserted on next S5->S0 transition. Rails will power-up as if from S3, but MEM_RESET_L will not properly assert. Software must deassert ISOLATE_CPU_MEM_L and then generate a valid reset cycle on CPU_MEM_RESET_L.


SYNCH MASTER-313 M16		SYNCH DATE-11/18/2015	
PRICE TITLE			
CPU Memory S3 Support			
 Apple Inc.		DRAWING NUMBER	051-9276
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		REVISION	2.7.0
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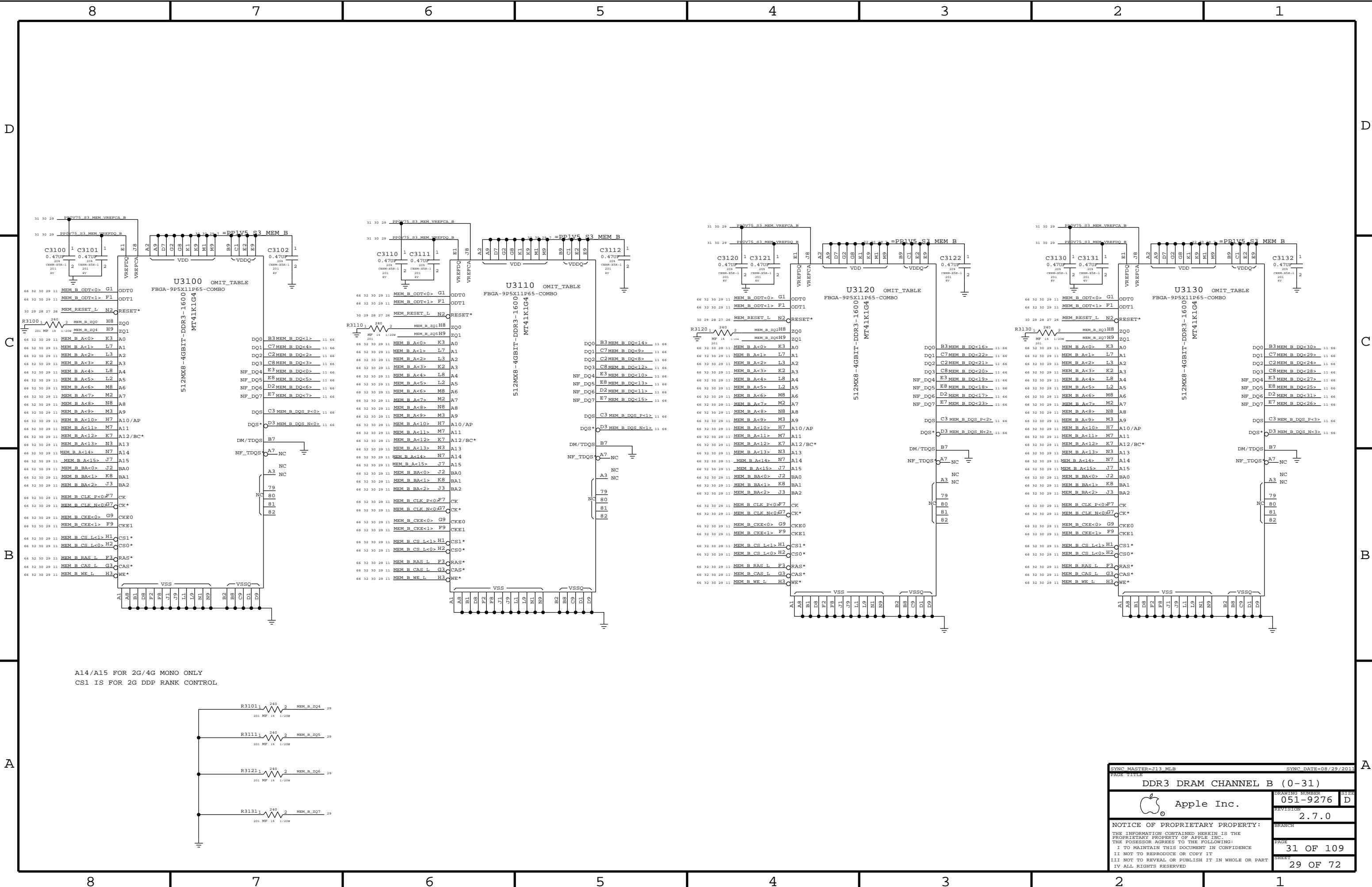




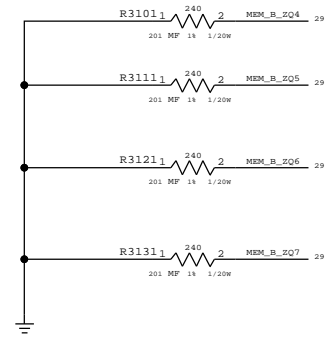
A14/A15 FOR 2G/4G MONO ONLY
CS1 IS FOR 2G DDP RANK CONTROL




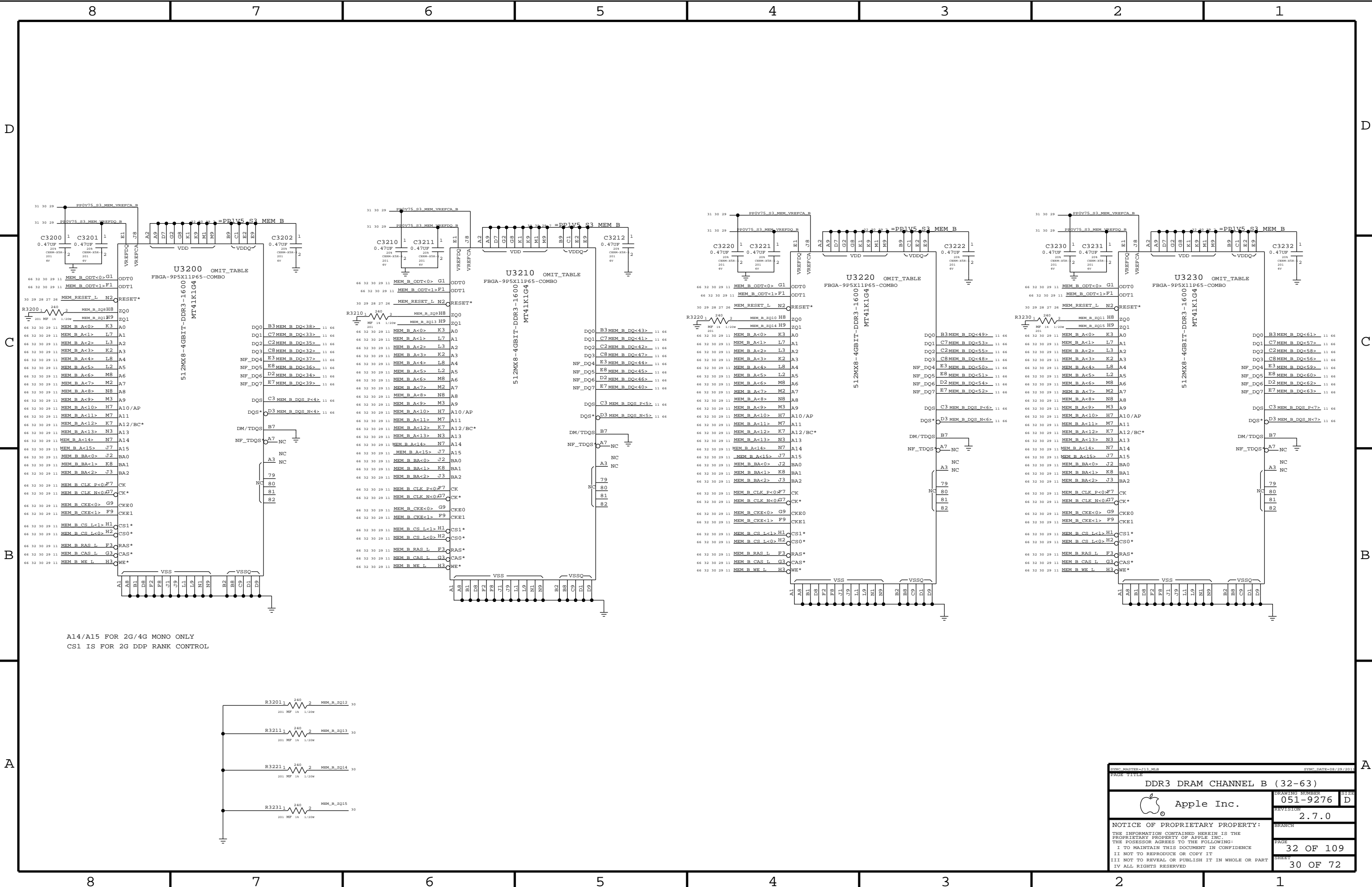
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DDR3 DRAM CHANNEL A (32-63)			
 Apple Inc.	DRAWING NUMBER	051-9276	SIZE D
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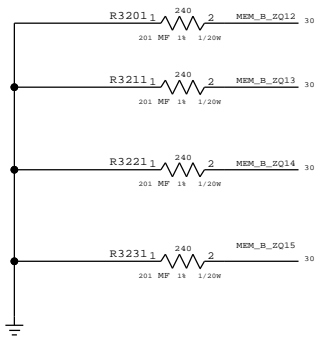
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CS1 IS FOR 2G DDP RANK CONTROL




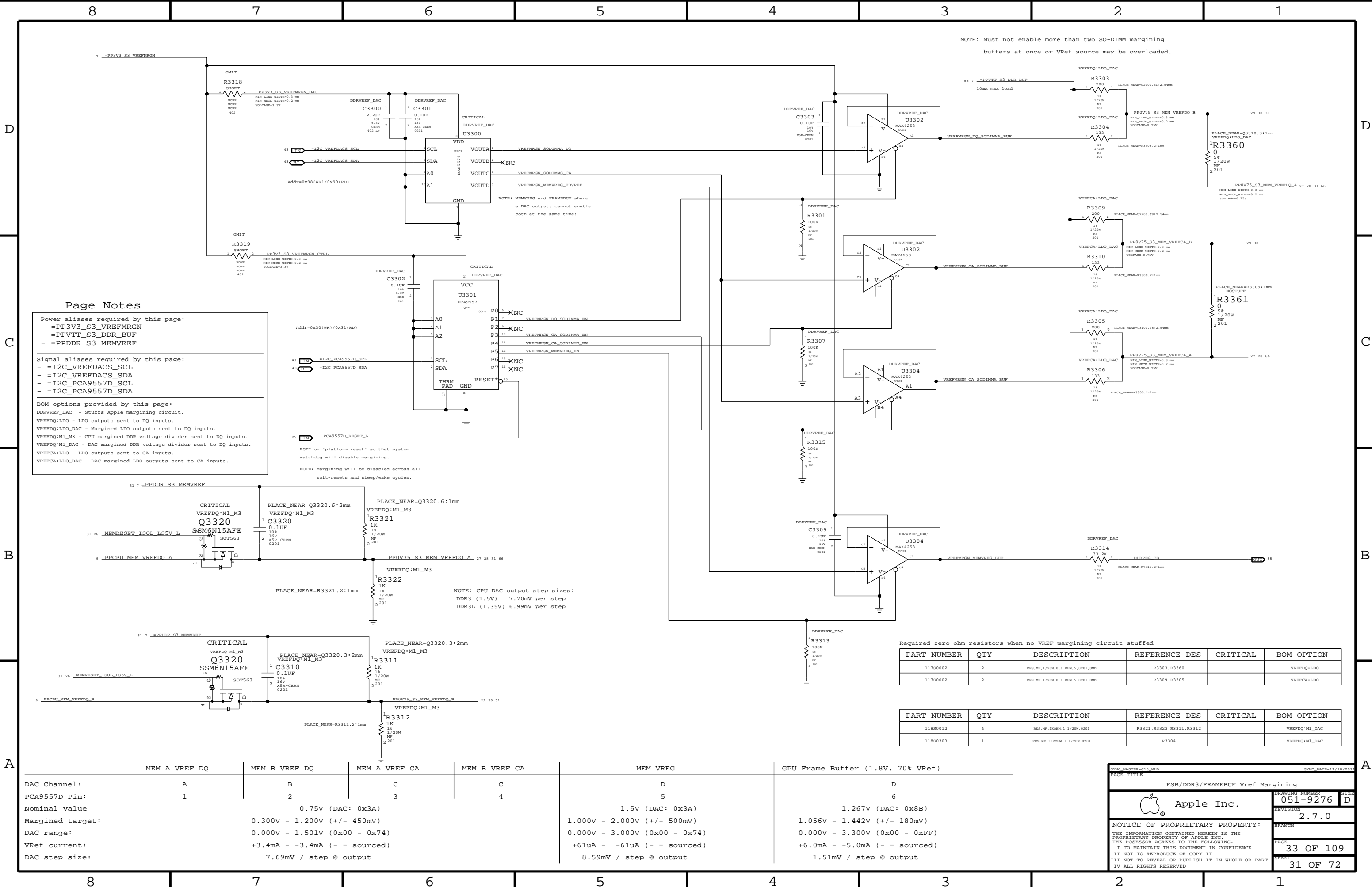
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PAGE TITLE			
DDR3 DRAM CHANNEL B (0-31)			
 Apple Inc.	DRAWING NUMBER	051-9276	SIZE D
	REVISION	2.7.0	
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CS1 IS FOR 2G DDP RANK CONTROL



SYMC PART#-U313 MEM		SYMC DATE-08/29/2011	
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DDR3 DRAM CHANNEL B (32-63)		DRAWING NUMBER	SIZE
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Page Notes

Power aliases required by this page:

- =PP3V3_S3_VREFMRGN
- =PPVTT_S3_DDR_BUF
- =PPDDR_S3_MEMVREF

Signal aliases required by this page:

- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:

- DDRREF_DAC - Stuffs Apple margining circuit.
- VREFDQ:LDO - LDO outputs sent to DQ inputs.
- VREFDQ:LDO_DAC - Margined LDO outputs sent to DQ inputs.
- VREFDQ:M1_M3 - CPU margined DDR voltage divider sent to DQ inputs.
- VREFDQ:M1_DAC - DAC margined DDR voltage divider sent to DQ inputs.
- VREFCA:LDO - LDO outputs sent to CA inputs.
- VREFCA:LDO_DAC - DAC margined LDO outputs sent to CA inputs.

NOTE: Margining will be disabled across all soft-resets and sleep/wake cycles.

NOTE: CPU DAC output step sizes:
DDR3 (1.5V) 7.70mV per step
DDR3L (1.35V) 6.99mV per step

Required zero ohm resistors when no VREF margining circuit stuffed

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
11780002	2	RES,MP,1/20W,0.0 OHM,5,0201,SMD	R3303,R3360		VREFDQ:LDO
11780002	2	RES,MP,1/20W,0.0 OHM,5,0201,SMD	R3309,R3305		VREFCA:LDO

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
11880012	4	RES,MP,1KOHM,1,1/20W,0201	R3321,R3322,R3311,R3312		VREFDQ:M1_DAC
11880003	1	RES,MP,3320OHM,1,1/20W,0201	R3304		VREFDQ:M1_DAC

	MEM A VREF DQ	MEM B VREF DQ	MEM A VREF CA	MEM B VREF CA	MEM VREG	GPU Frame Buffer (1.8V, 70% Vref)
DAC Channel:	A	B	C	C	D	D
PCA9557D Pin:	1	2	3	4	5	6
Nominal value		0.75V (DAC: 0x3A)			1.5V (DAC: 0x3A)	1.267V (DAC: 0x8B)
Margined target:		0.300V - 1.200V (+/- 450mV)			1.000V - 2.000V (+/- 500mV)	1.056V - 1.442V (+/- 180mV)
DAC range:		0.000V - 1.501V (0x00 - 0x74)			0.000V - 3.000V (0x00 - 0xFF)	0.000V - 3.300V (0x00 - 0xFF)
VRef current:		+3.4mA - -3.4mA (- = sourced)			+61uA - -61uA (- = sourced)	+6.0mA - -5.0mA (- = sourced)
DAC step size:		7.69mV / step @ output			8.59mV / step @ output	1.51mV / step @ output

SYMC PARTSHEET:113 WEB SYMC DATE:11/18/2011

FSB/DDR3/FRAMEBUF Vref Margining

Apple Inc.

051-9276

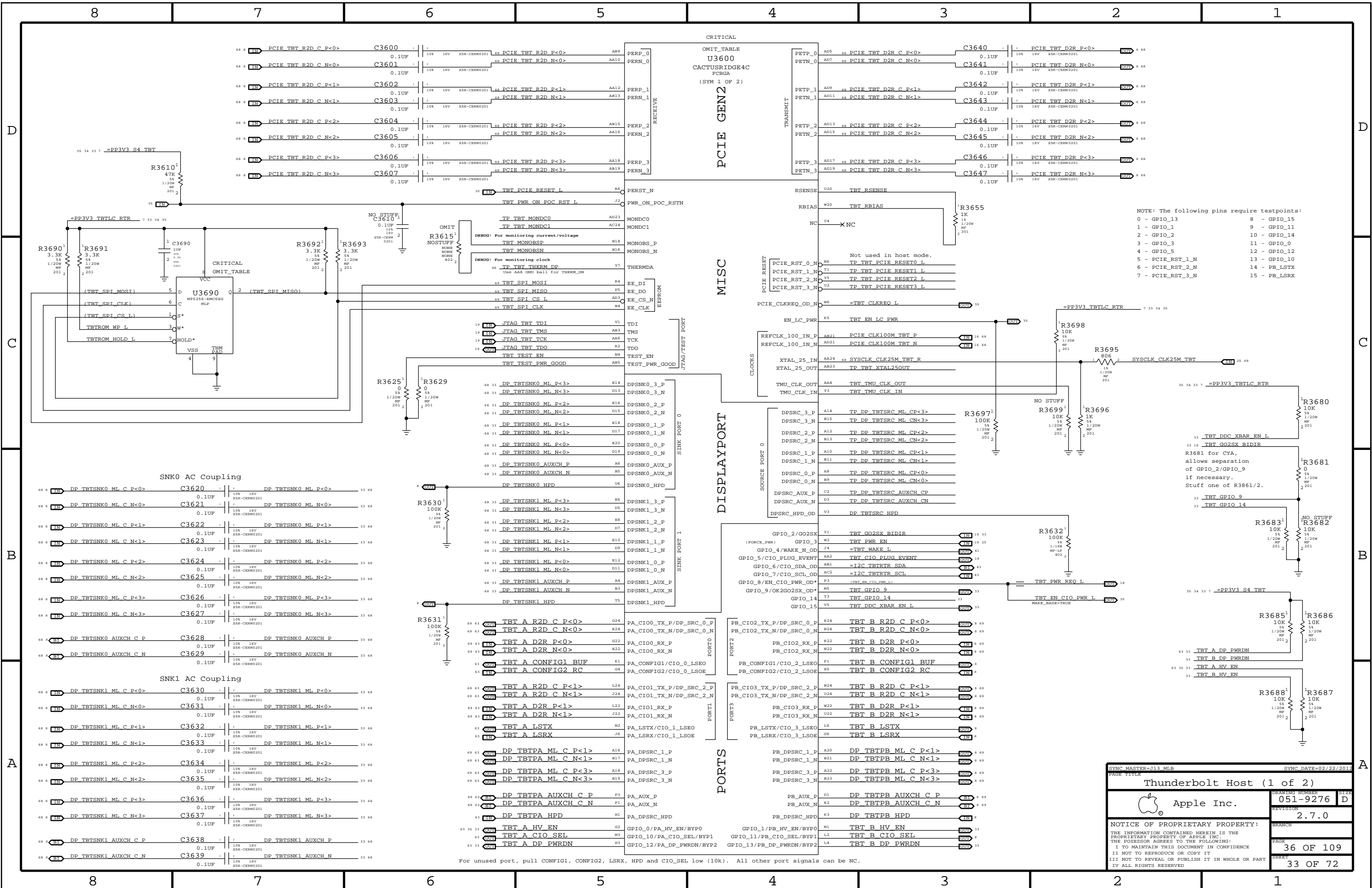
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SYNC MASTER=J13 MLB

SYNC DATE=03/22/2012

Thunderbolt Host (1 of 2)

Apple Inc.

DRAWING NUMBER
051-9276

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```

Power aliases required by this page:
- =PPVIN_SW_TBTBST      (8-13V Boost Input)
- =PP18V_TBT_REG        (18V Boost Output)
- =PP3V3_TBT_P3V3TBTFT (1.3V FET Input)
- =PP3V3_TBT_FET        (3.3V FET Output)
- =PP3V3_S0_TBT_PMRCTL
- =PP1V05_TBT_P1V05TBTFT (1.05V FET Input)
- =PP1V05_TBT_FET       (1.05V FET Output)

```

```

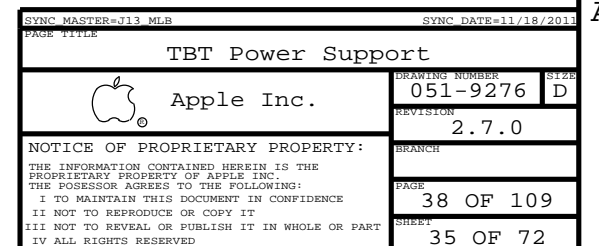
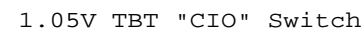
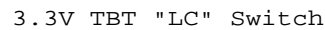
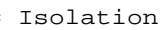
Signal aliases required by this page:
- =TBT_CLKREQ_L
- =TBT_RESET_L

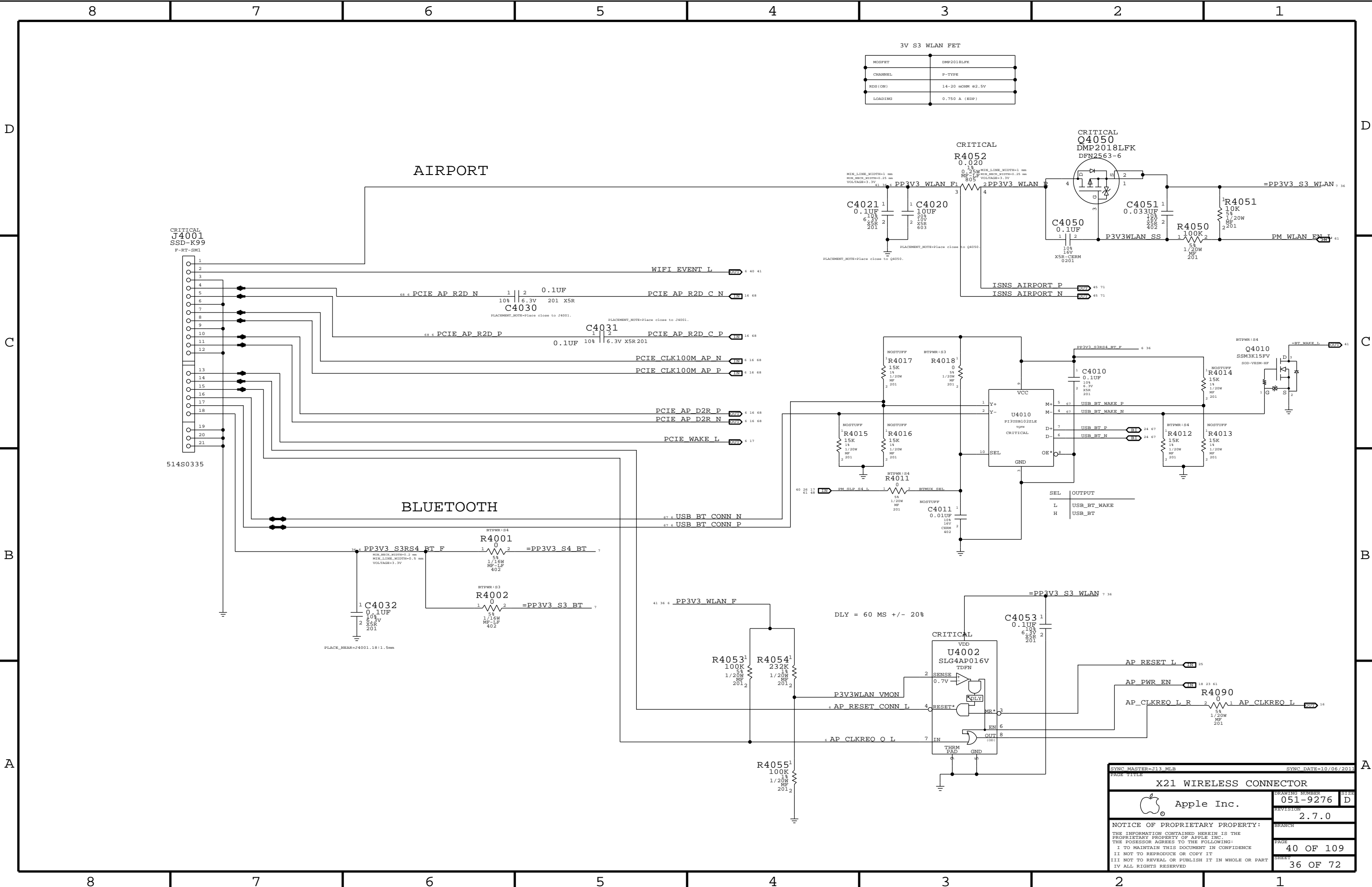
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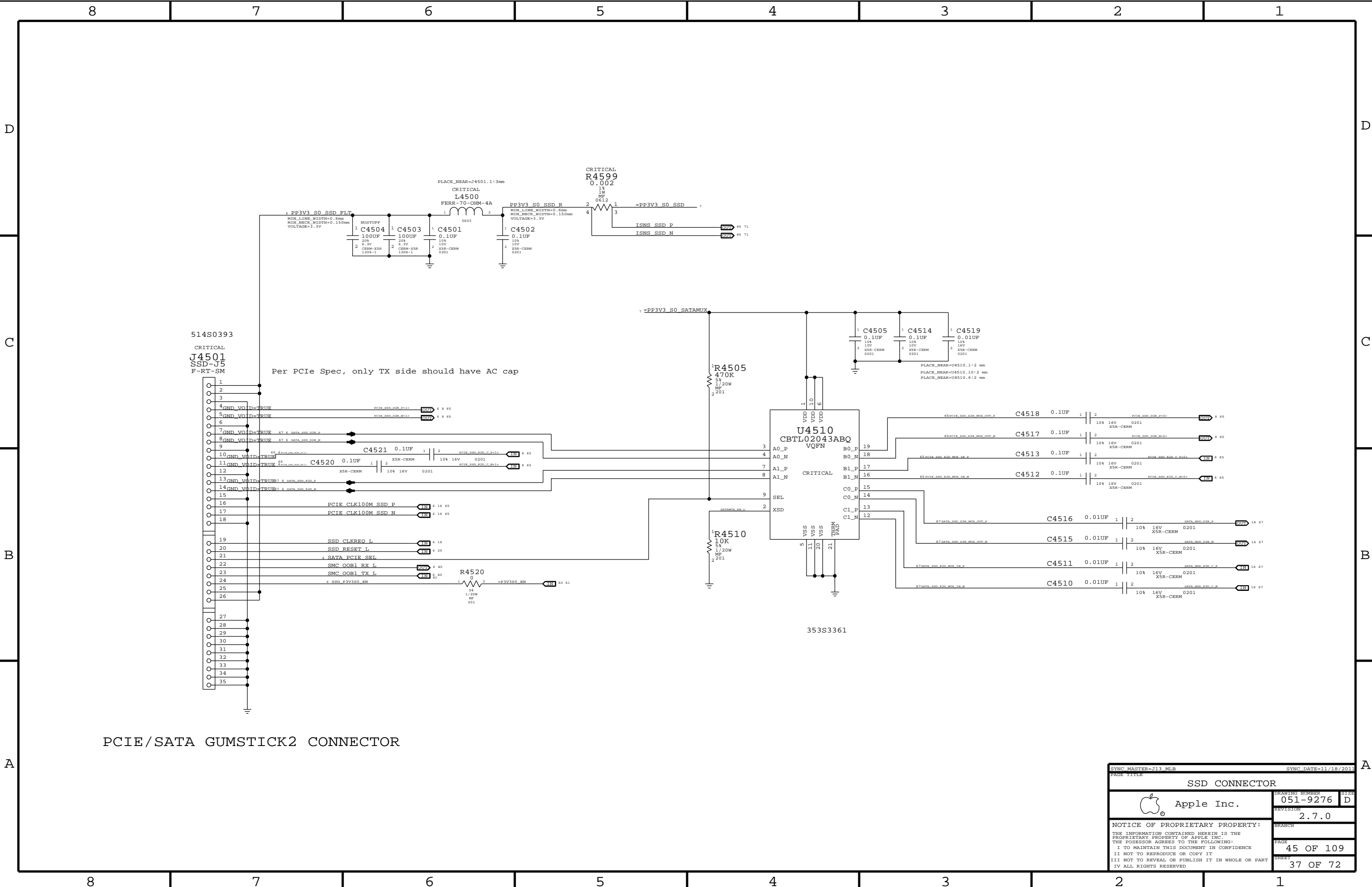
BOM options provided by this page:
TBTBST:Y - Stuffs 18V boost circuitry.

```






SYNC MASTER=J13 MLB		SYNC DATE=10/06/2011	
PAGE TITLE		X21 WIRELESS CONNECTOR	
DRAWING NUMBER		051-9276	SIZE D
REVISION		2.7.0	BRANCH
PAGE		40 OF 109	SHEET
SHEET		36 OF 72	

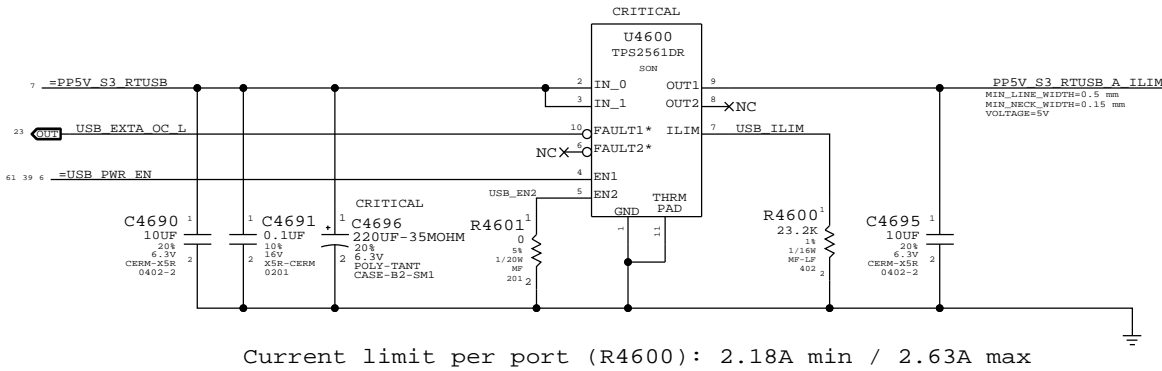


PCIE/SATA GUMSTICK2 CONNECTOR

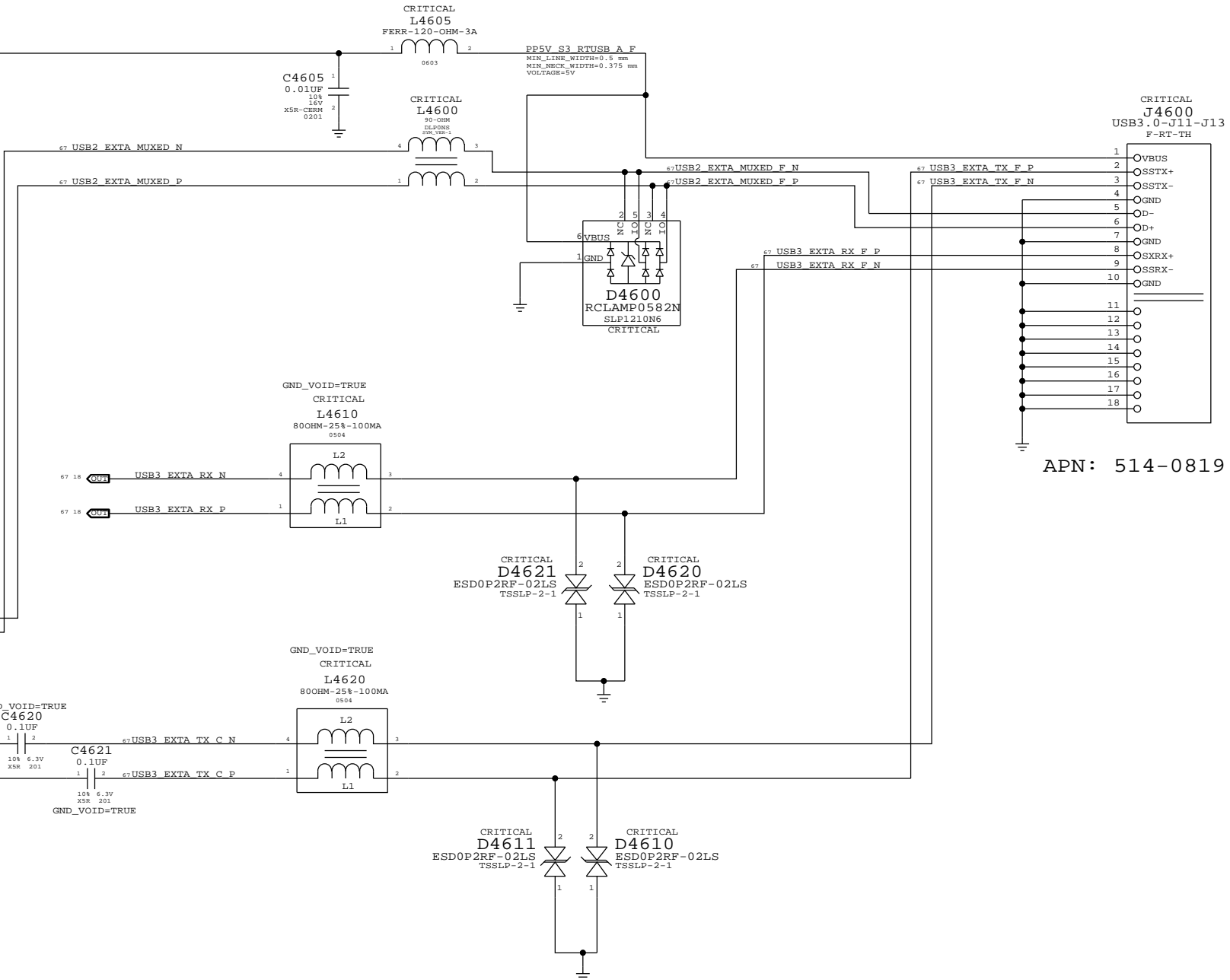
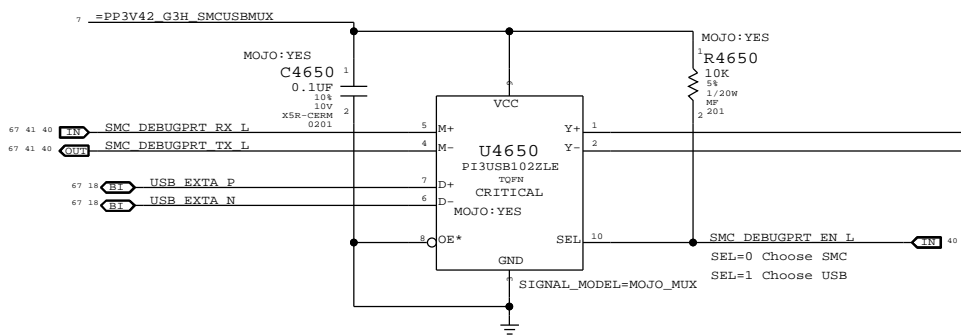
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 Apple Inc.		DRAWING NUMBER	051-9276
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Right USB Port A


USB Port Power Switch

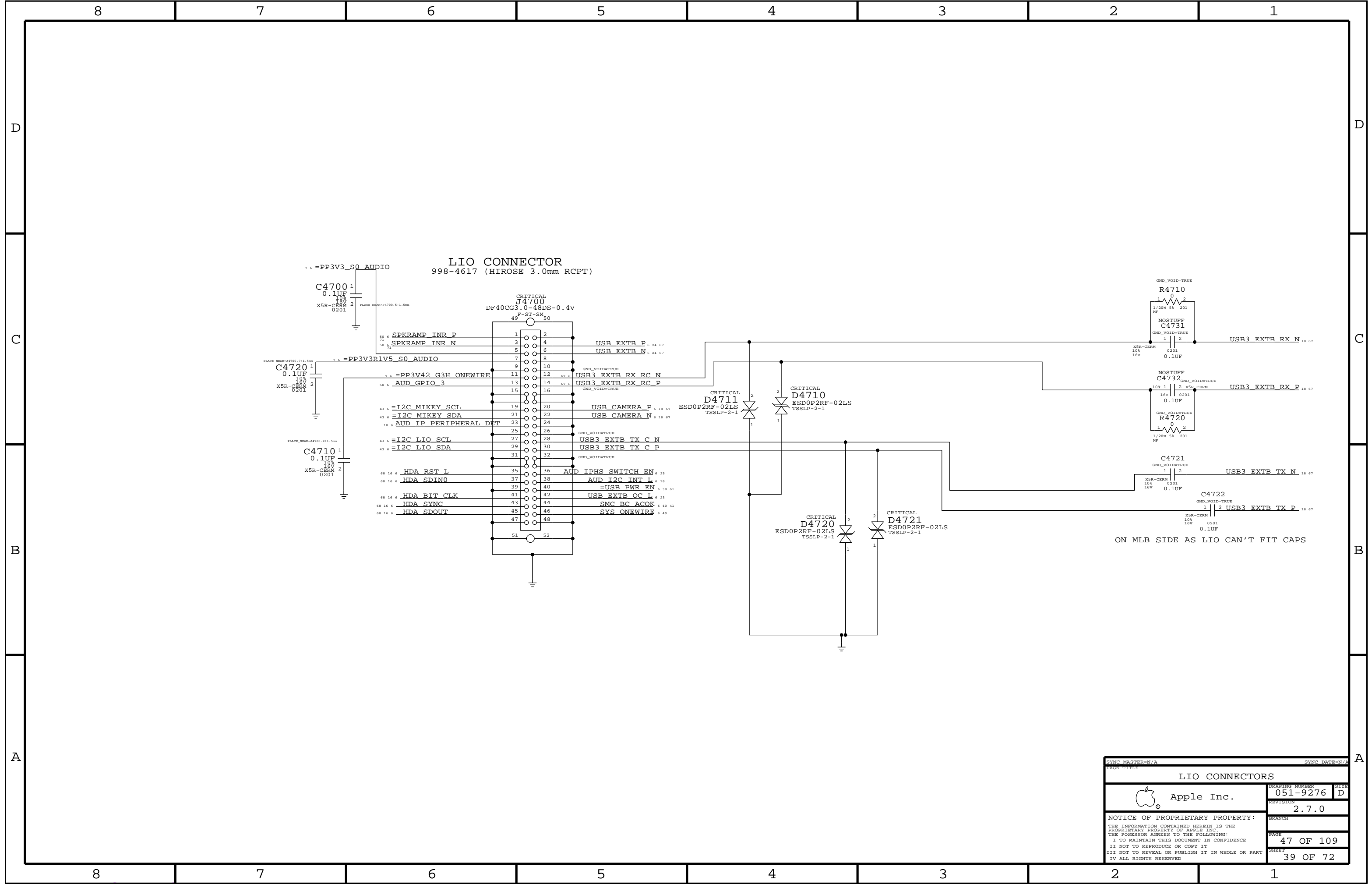



Mojo SMC Debug Mux



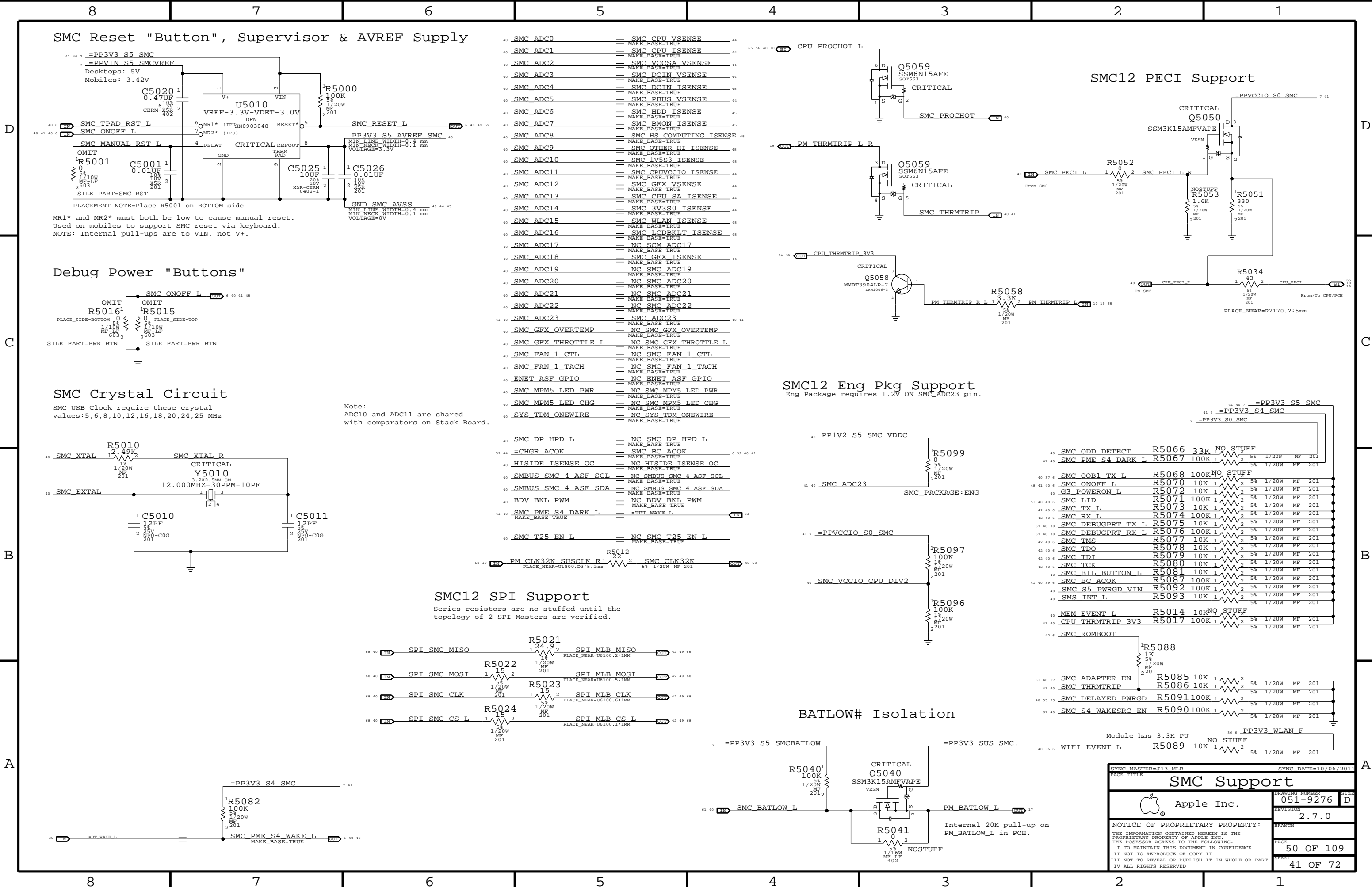
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External A USB3 Connector			
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		SIZE	D
		REVISION	2.7.0
		BRANCH	
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PAGE TITLE			
LIO CONNECTORS			
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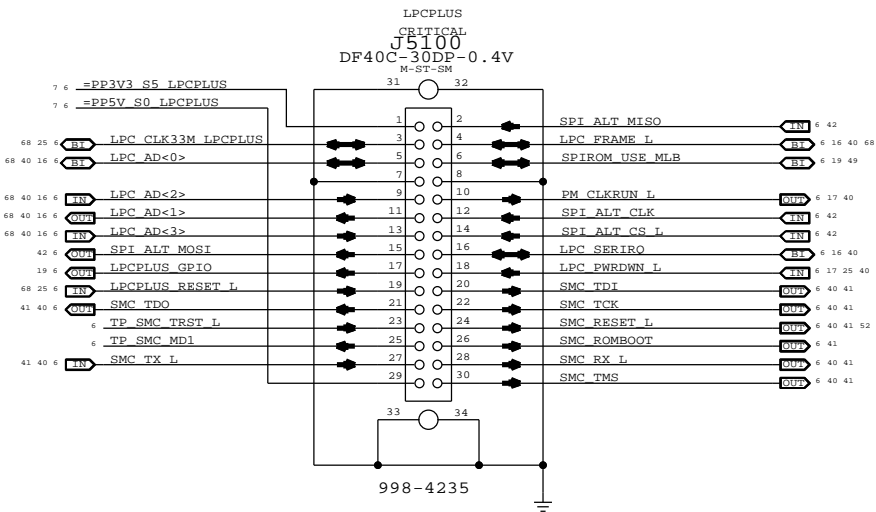
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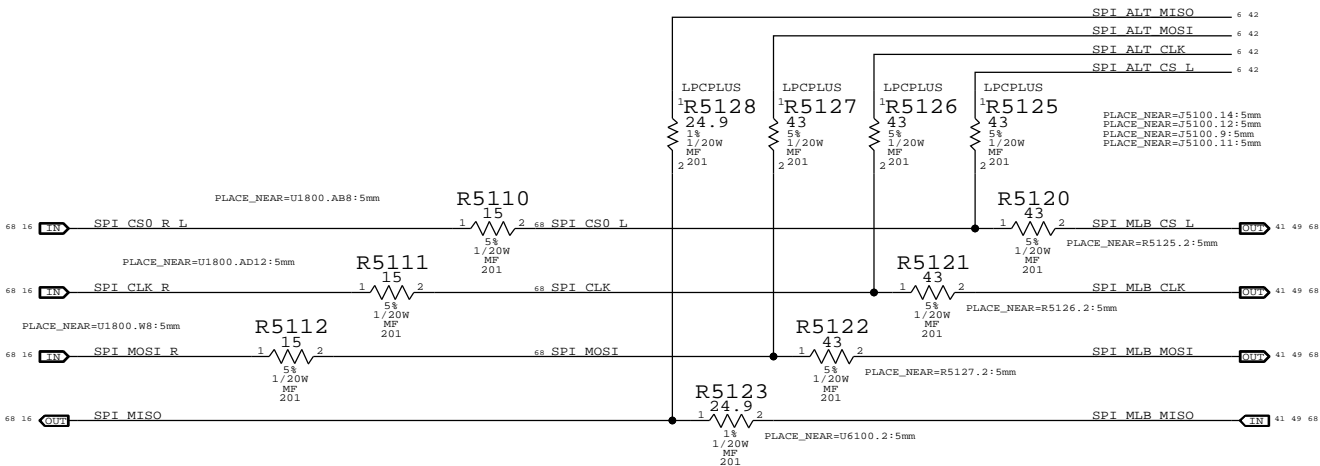
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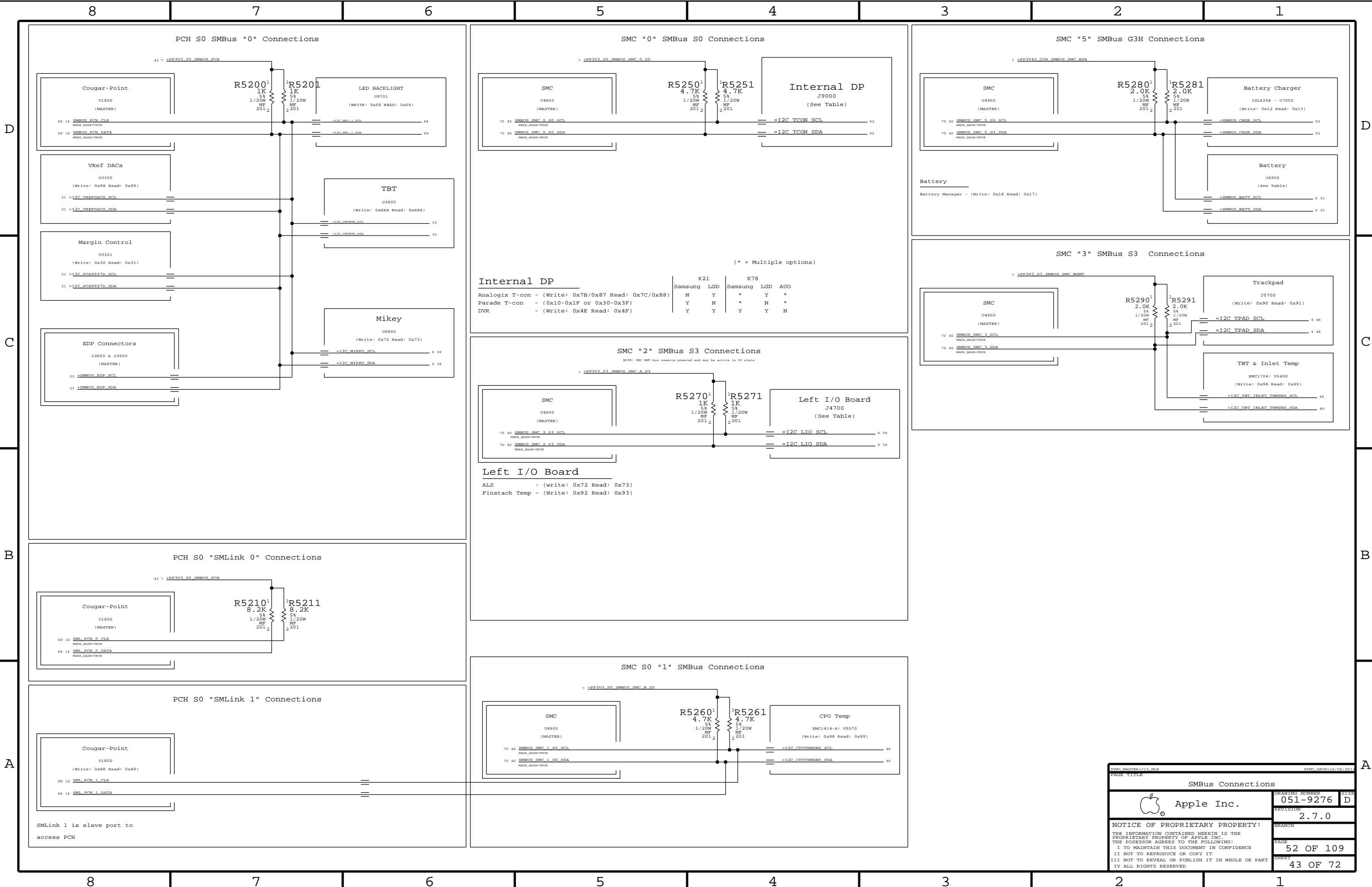
LPC+SPI Connector



SPI Bus Series Termination



SYNC MASTER=K21 MLB		SYNC DATE=12/13/2010	
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LPC+SPI Debug Connector			
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SYMC MASTER=113 MCB

SYMC DATE=10/09/2011

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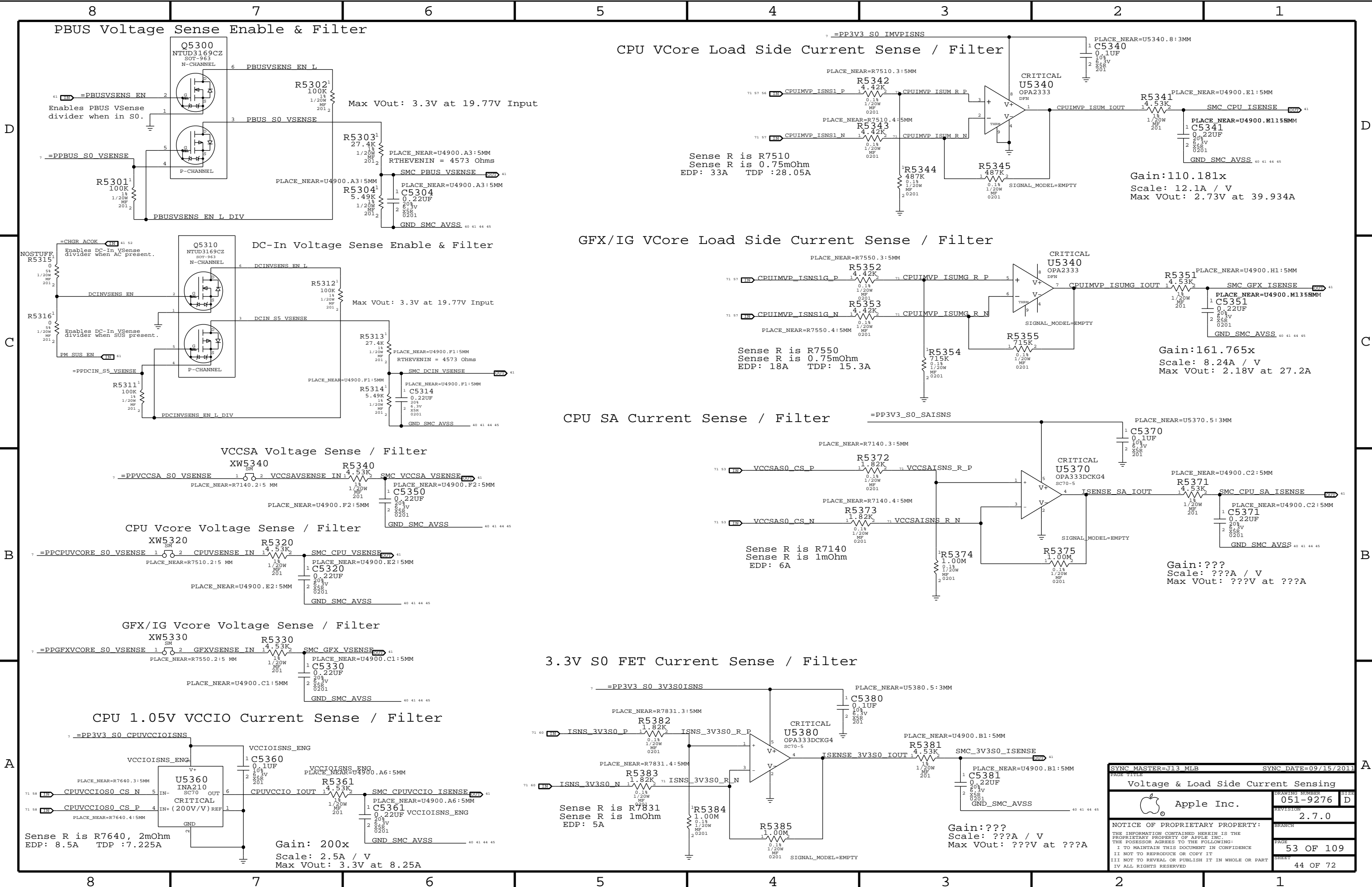
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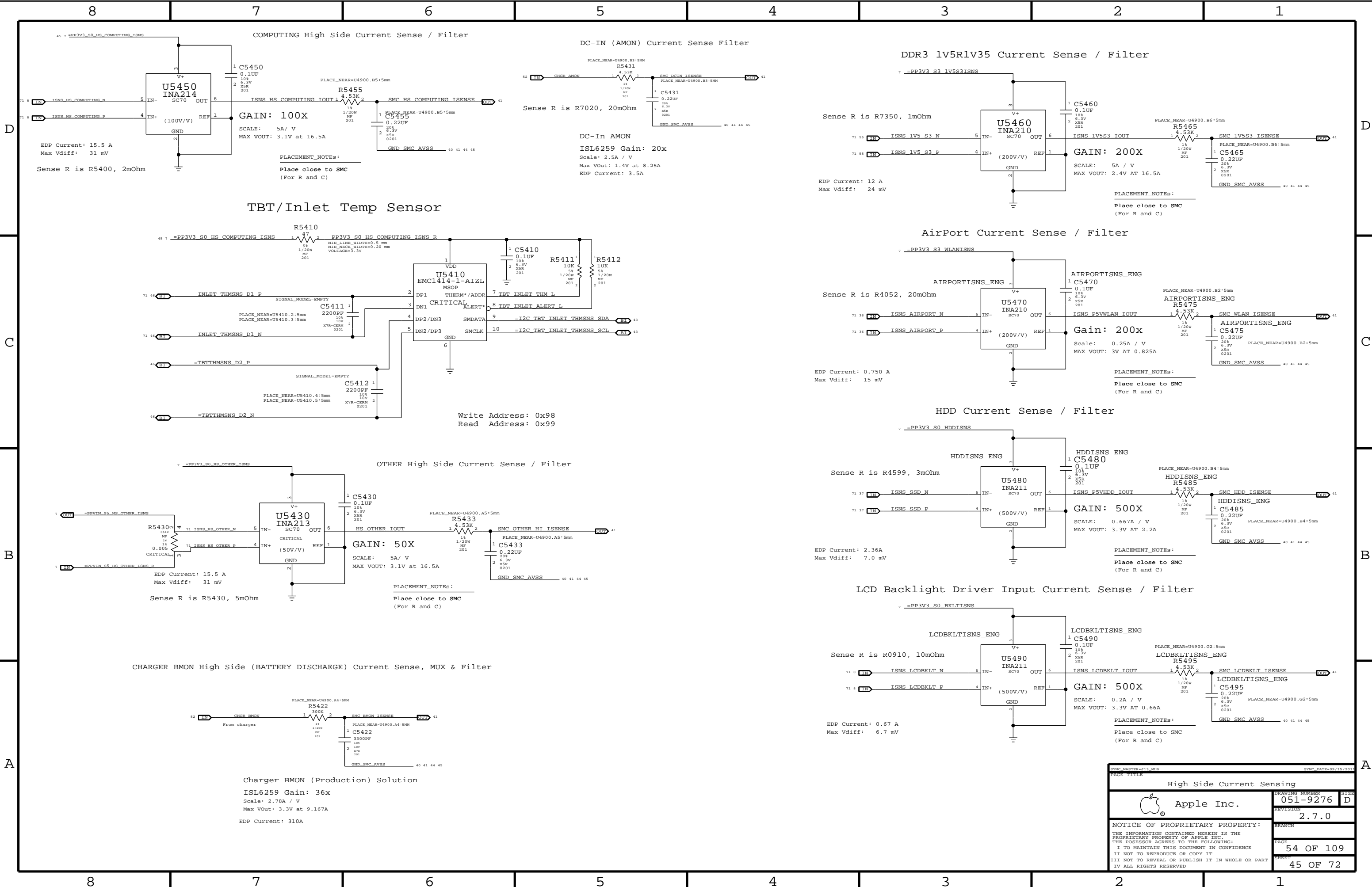
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PAGE TITLE			
Voltage & Load Side Current Sensing			
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			051-9276
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		2.7.0	
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SYMC MASTER=113 MLE		SYMC DATE=09/15/2011	
PAGE TITLE			
High Side Current Sensing		DRAWING NUMBER	SIZE
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CPU Proximity Sensor

Detect CPU Die Temperature

Detect DDR/5V/3.3V Proximity Temperature

Placement note:
Place U5510 under CPU

Write Address: 0x98
Read Address: 0x99

TBT Die

Replacing caps with 100K PD on ISENSE SMC inputs

TBT,MLB Bottom & Inlet Proximity Sensors

Part Number

Qty

Description

Reference Des

Critical

BOM Option

117S0008

1

RES,MF,1/20W,100K OHM,5,0201,SMD

C5361

VCCIOISNS_PROD

117S0008

1

RES,MF,1/20W,100K OHM,5,0201,SMD

C5475

AIRPORTISNS_PROD

117S0008

1

RES,MF,1/20W,100K OHM,5,0201,SMD

C5485

HDDISNS_PROD

117S0008

1

RES,MF,1/20W,100K OHM,5,0201,SMD

C5495

LCDCLKTISNS_PROD

Sync Master=J13 MLB

Sync Date=08/30/2013

Page Title

Thermal Sensors

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051-9276

Revision

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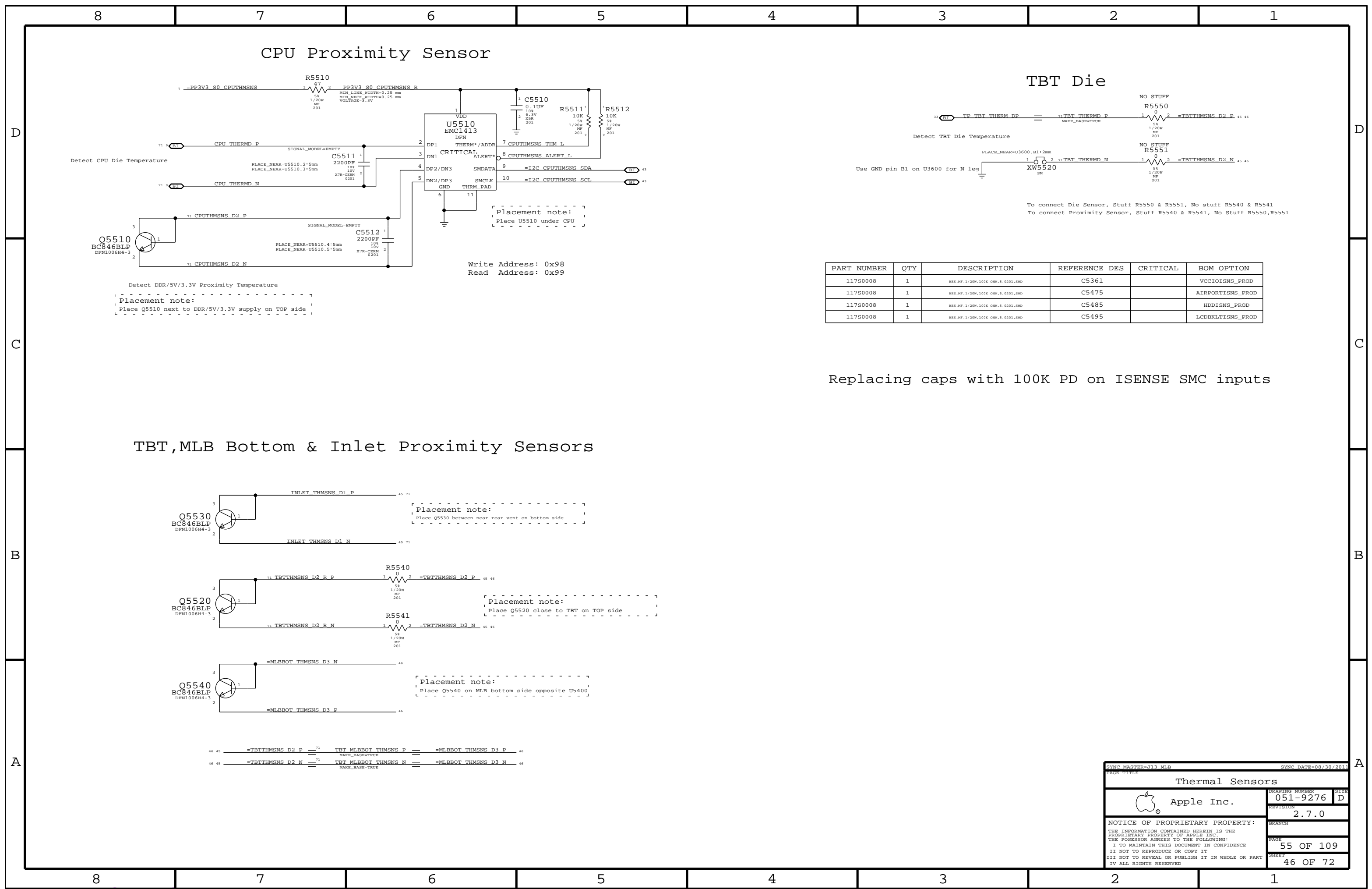
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[illegible][illegible]

CPU Proximity Sensor

Detect CPU Die Temperature

Detect DDR/5V/3.3V Proximity Temperature

Placement note:
Place U5510 under CPU

Write Address: 0x98
Read Address: 0x99

TBT Die

Replacing caps with 100K PD on ISENSE SMC inputs

TBT,MLB Bottom & Inlet Proximity Sensors

Part Number

Qty

Description

Reference Des

Critical

BOM Option

117S0008

1

RES,MF,1/20W,100K OHM,5,0201,SMD

C5361

VCCIOISNS_PROD

117S0008

1

RES,MF,1/20W,100K OHM,5,0201,SMD

C5475

AIRPORTISNS_PROD

117S0008

1

RES,MF,1/20W,100K OHM,5,0201,SMD

C5485

HDDISNS_PROD

117S0008

1

RES,MF,1/20W,100K OHM,5,0201,SMD

C5495

LCDCLKTISNS_PROD

Sync Master=J13 MLB

Sync Date=08/30/2013

Page Title

Thermal Sensors

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Sheet

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CPU Proximity Sensor

Detect CPU Die Temperature

Detect DDR/5V/3.3V Proximity Temperature

Placement note:
Place U5510 under CPU

Write Address: 0x98
Read Address: 0x99

TBT Die

Detect TBT Die Temperature

Use GND pin B1 on U3600 for N leg

To connect Die Sensor, Stuff R5550 & R5551, No stuff R5540 & R5541
To connect Proximity Sensor, Stuff R5540 & R5541, No Stuff R5550,R5551

Replacing caps with 100K PD on ISENSE SMC inputs

TBT,MLB Bottom & Inlet Proximity Sensors

Placement note:
Place Q5530 between rear vent on bottom side

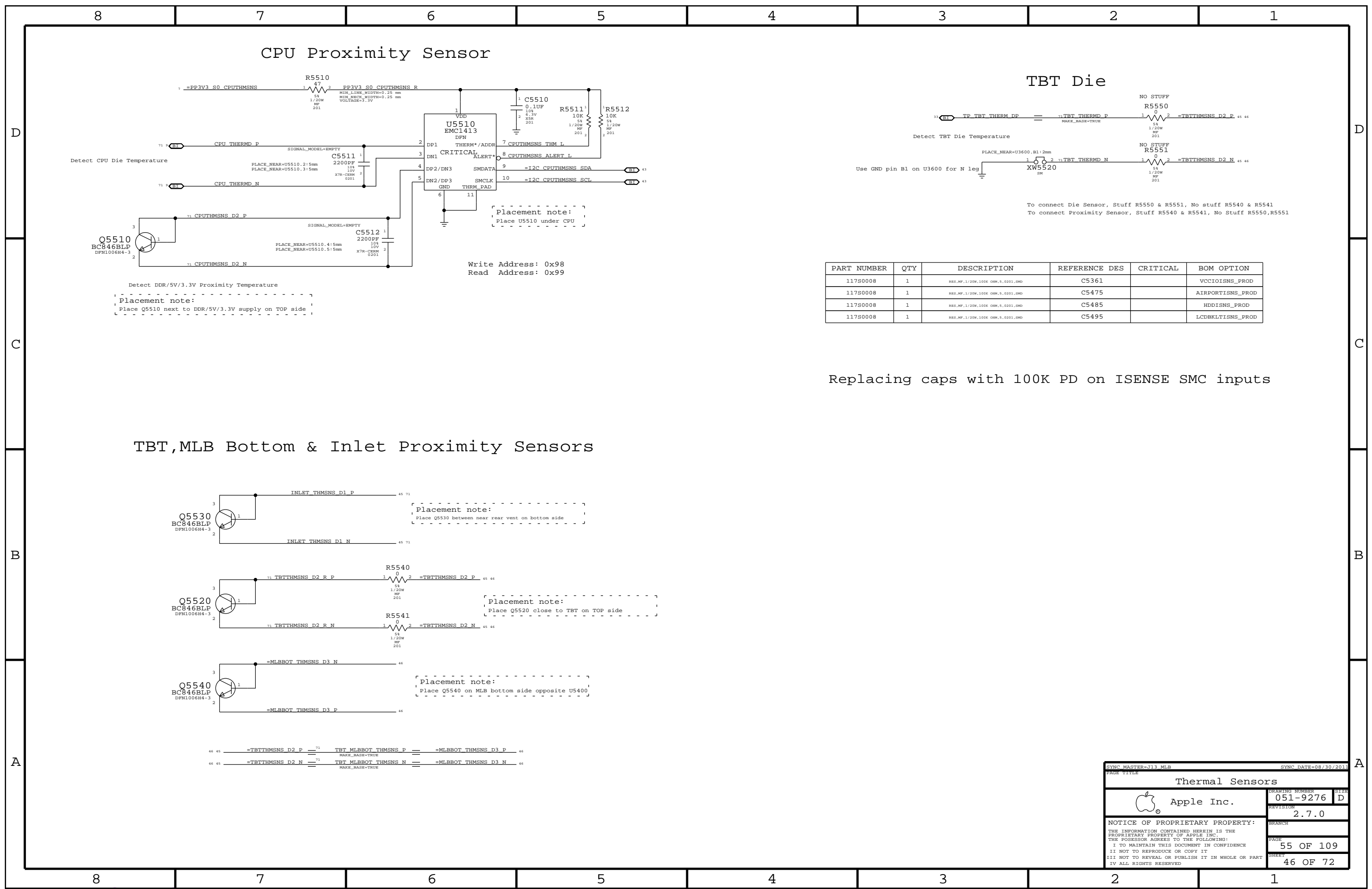
Placement note:
Place Q5520 close to TBT on TOP side

Placement note:
Place Q5540 on MLB bottom side opposite U5400

Thermal Sensors

Apple Inc.

NOTICE OF PROPRIETARY PROPERTY:



CPU Proximity Sensor

Detect CPU Die Temperature

Detect DDR/5V/3.3V Proximity Temperature

Placement note:
Place U5510 under CPU

Write Address: 0x98
Read Address: 0x99

TBT Die

Detect TBT Die Temperature

Use GND pin B1 on U3600 for N leg

To connect Die Sensor, Stuff R5550 & R5551, No stuff R5540 & R5541
To connect Proximity Sensor, Stuff R5540 & R5541, No Stuff R5550,R5551

Replacing caps with 100K PD on ISENSE SMC inputs

TBT,MLB Bottom & Inlet Proximity Sensors

Placement note:
Place Q5530 between rear vent on bottom side

Placement note:
Place Q5520 close to TBT on TOP side

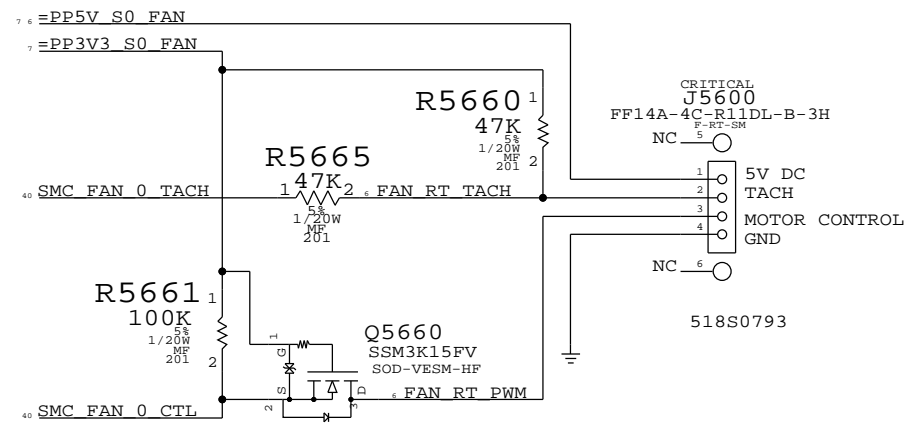
Placement note:
Place Q5540 on MLB bottom side opposite U5400

Thermal Sensors

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NOTICE OF PROPRIETARY PROPERTY:

FAN CONNECTOR



SYNC MASTER=K21 MLB		SYNC DATE=12/13/2010	
PAGE TITLE		Fan	
Apple Inc.		DRAWING NUMBER	051-9276
		REVISION	2.7.0
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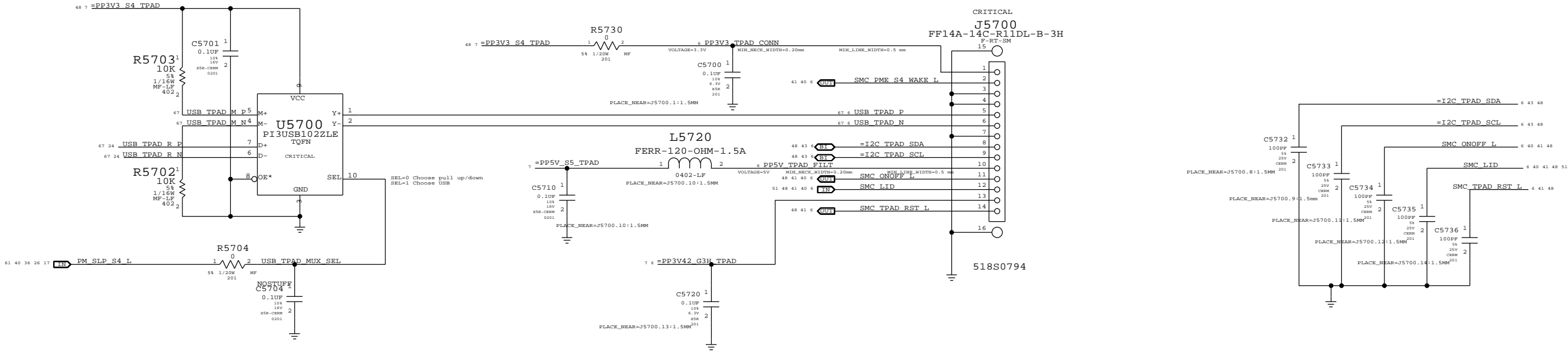
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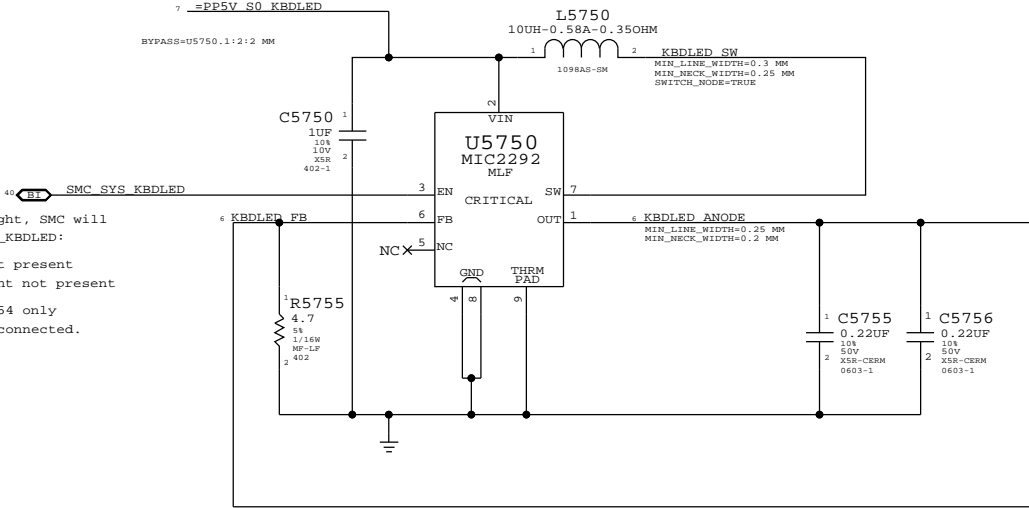
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IPD Flex Connector

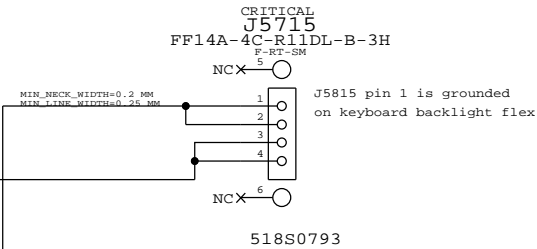



Keyboard Backlight Driver & Detection

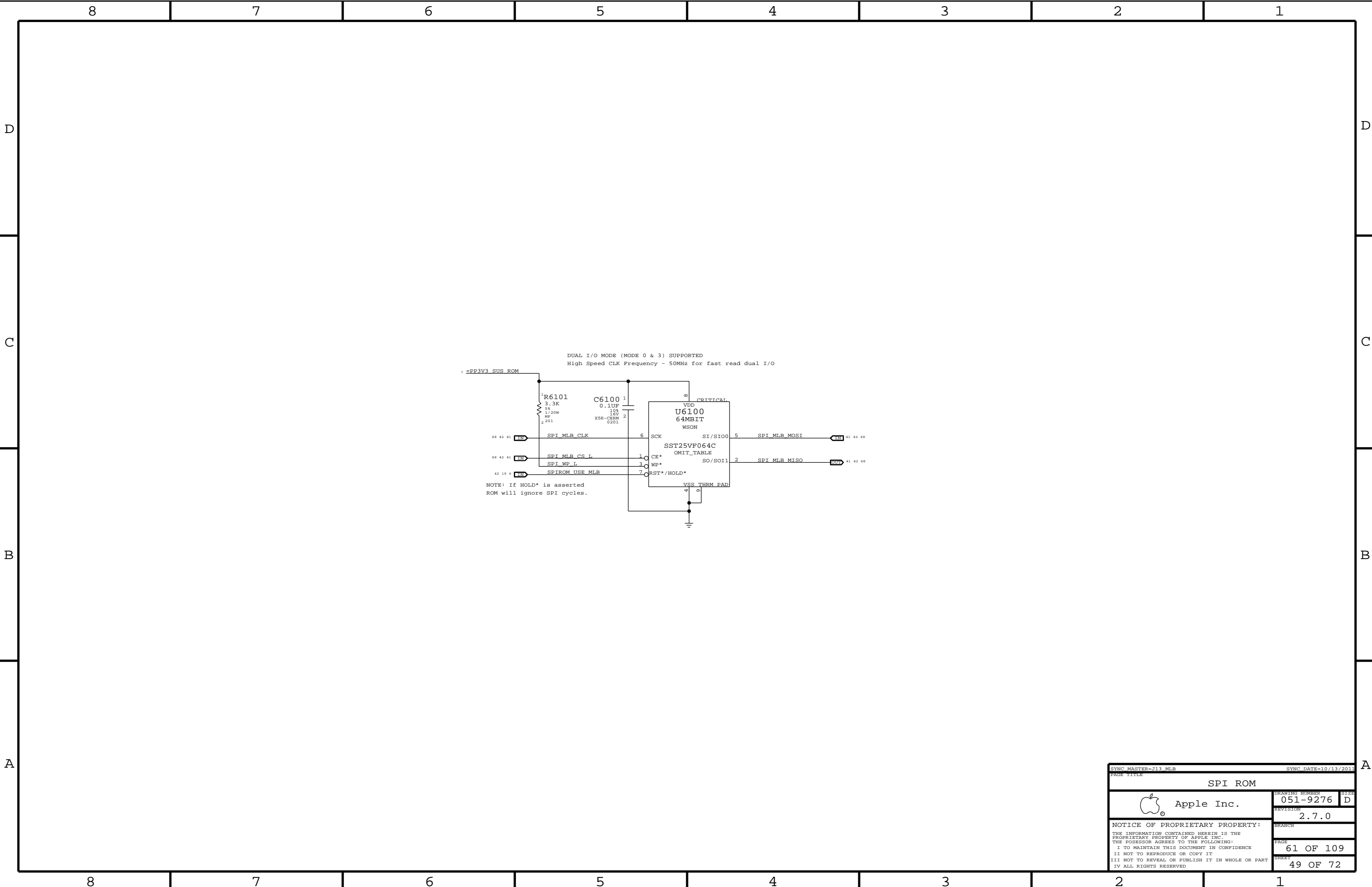
To detect Keyboard backlight, SMC will tristate and read SMC_SYS_KBDLED:
If LOW, keyboard backlight present
If HIGH, keyboard backlight not present
R5853 always stuffed, R5854 only grounded when KB BL flex connected.




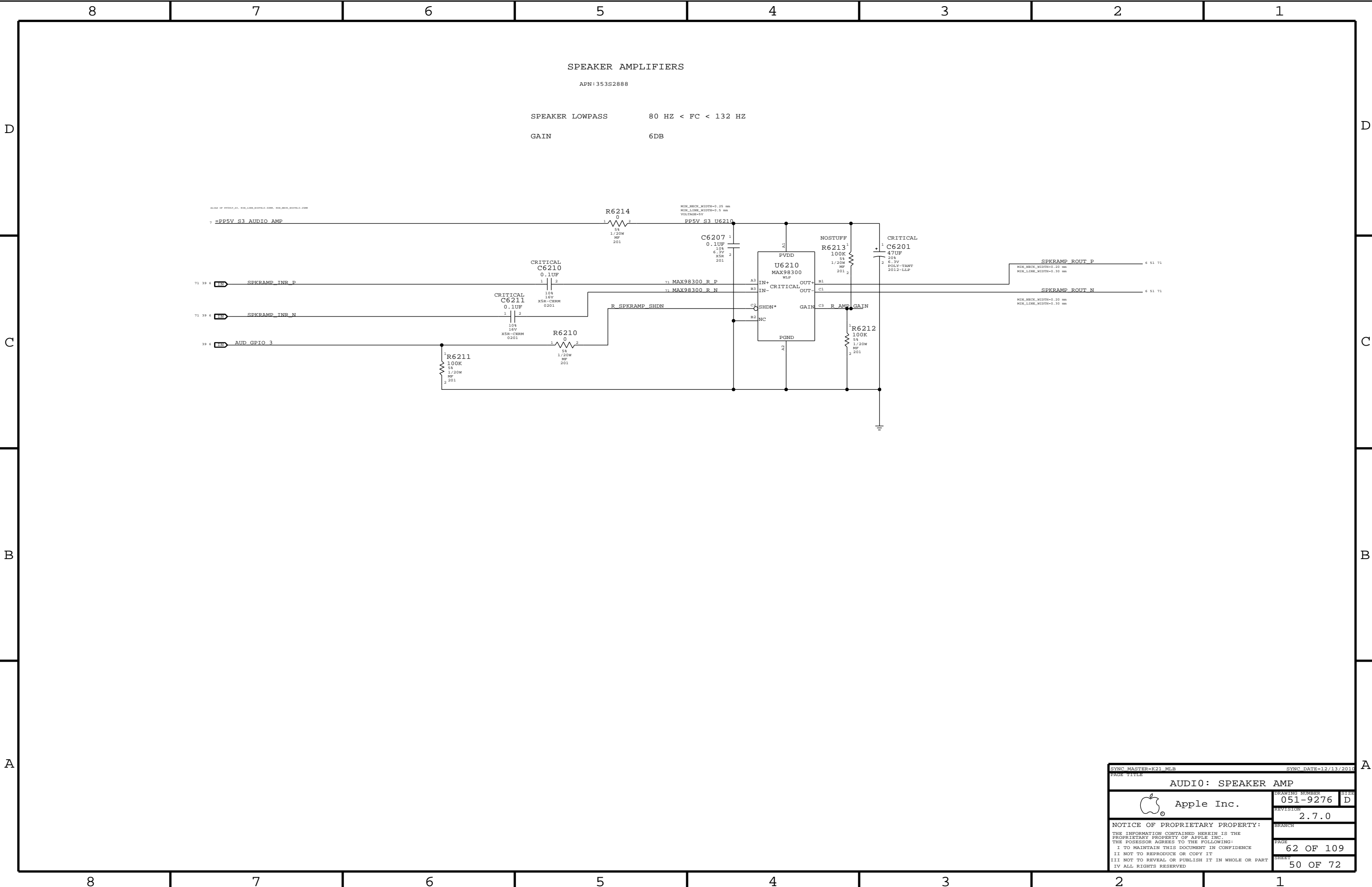
Keyboard Backlight Connector



SYNC MASTER=K21 MLB		SYNC DATE=12/13/2010	
PAGE TITLE			
IPD / KBD Backlight			
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		SIZE	D
		REVISION	2.7.0
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PAGE TITLE			
SPI ROM			
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SYNC MASTER=K21 MLB

SYNC DATE=12/13/2010

AUDIO0: SPEAKER AMP

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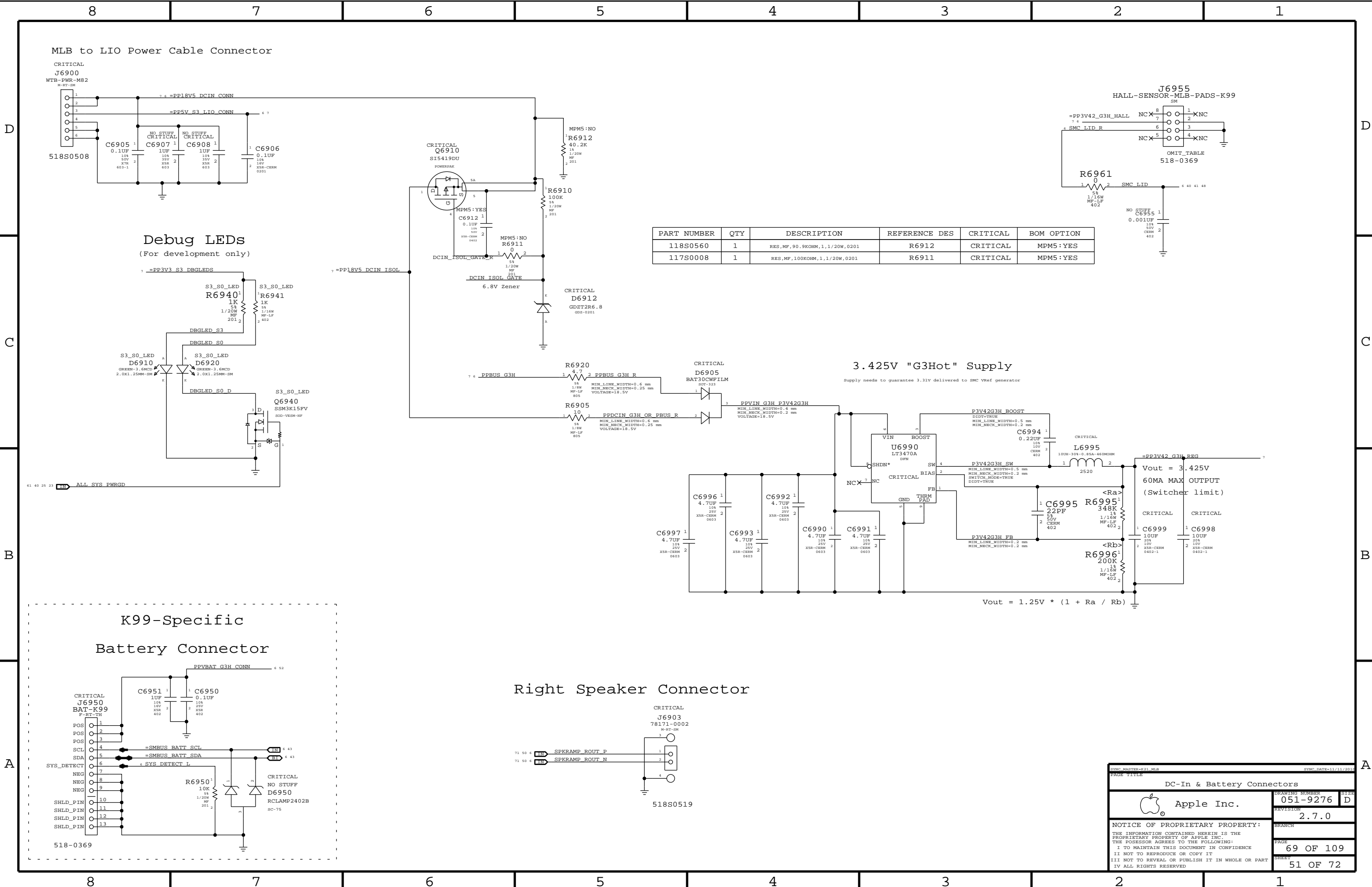
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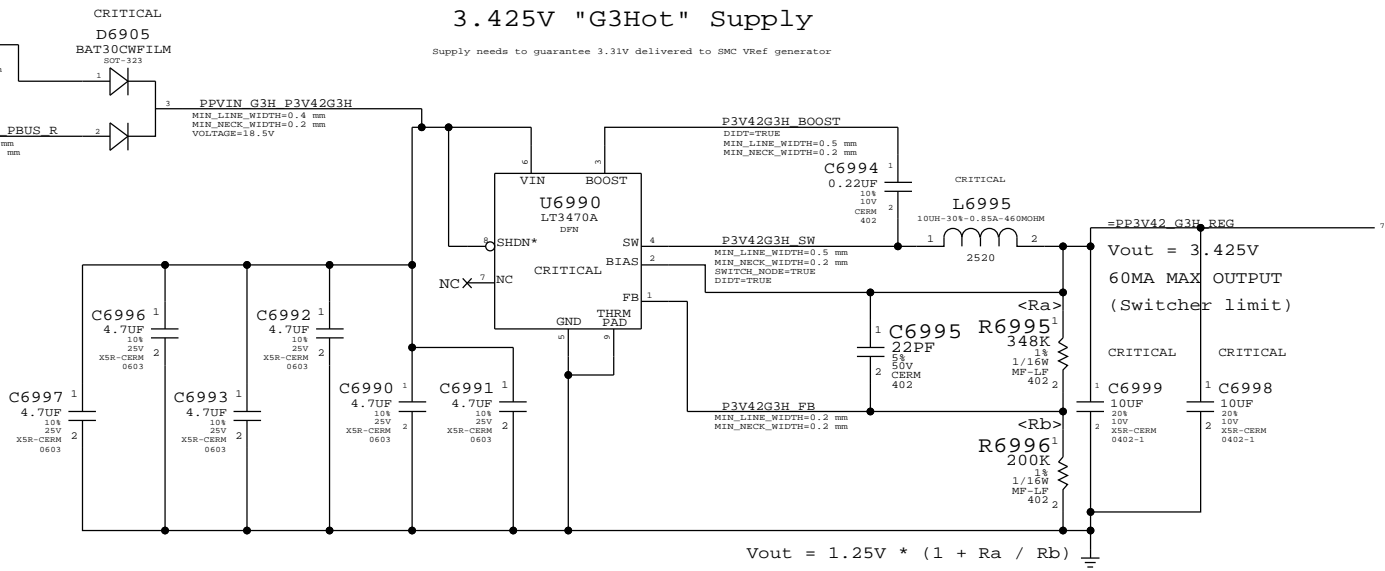
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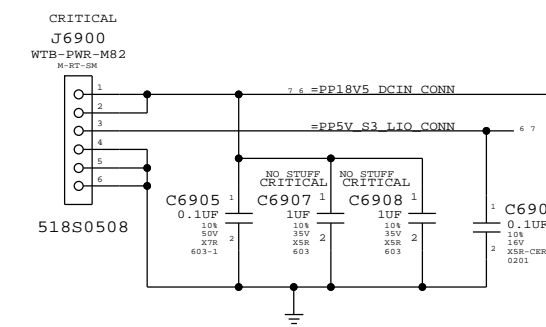
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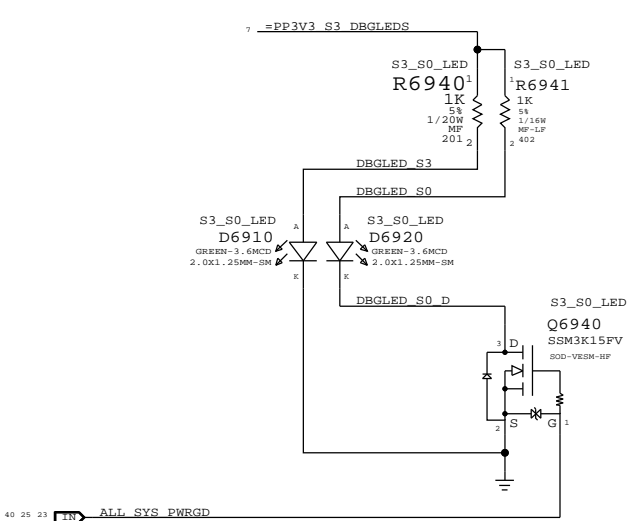
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0560	1	RES, MF, 90.9KOHM, 1, 1/20W, 0201	R6912	CRITICAL	MPM5: YES
117S0008	1	RES, MF, 100KOHM, 1, 1/20W, 0201	R6911	CRITICAL	MPM5: YES



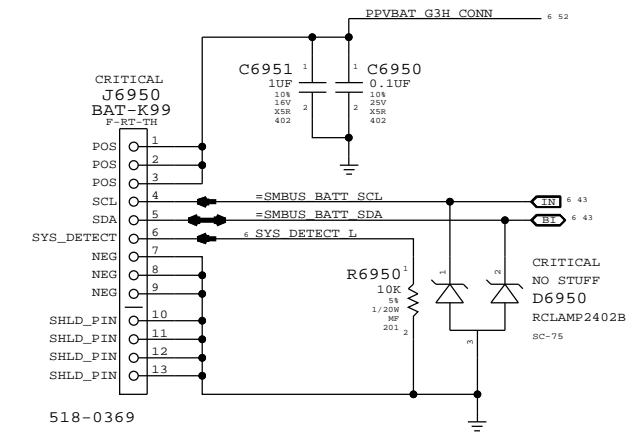
MLB to LIO Power Cable Connector



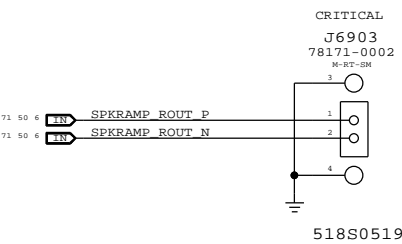
Debug LEDs
(For development only)



K99-Specific
Battery Connector

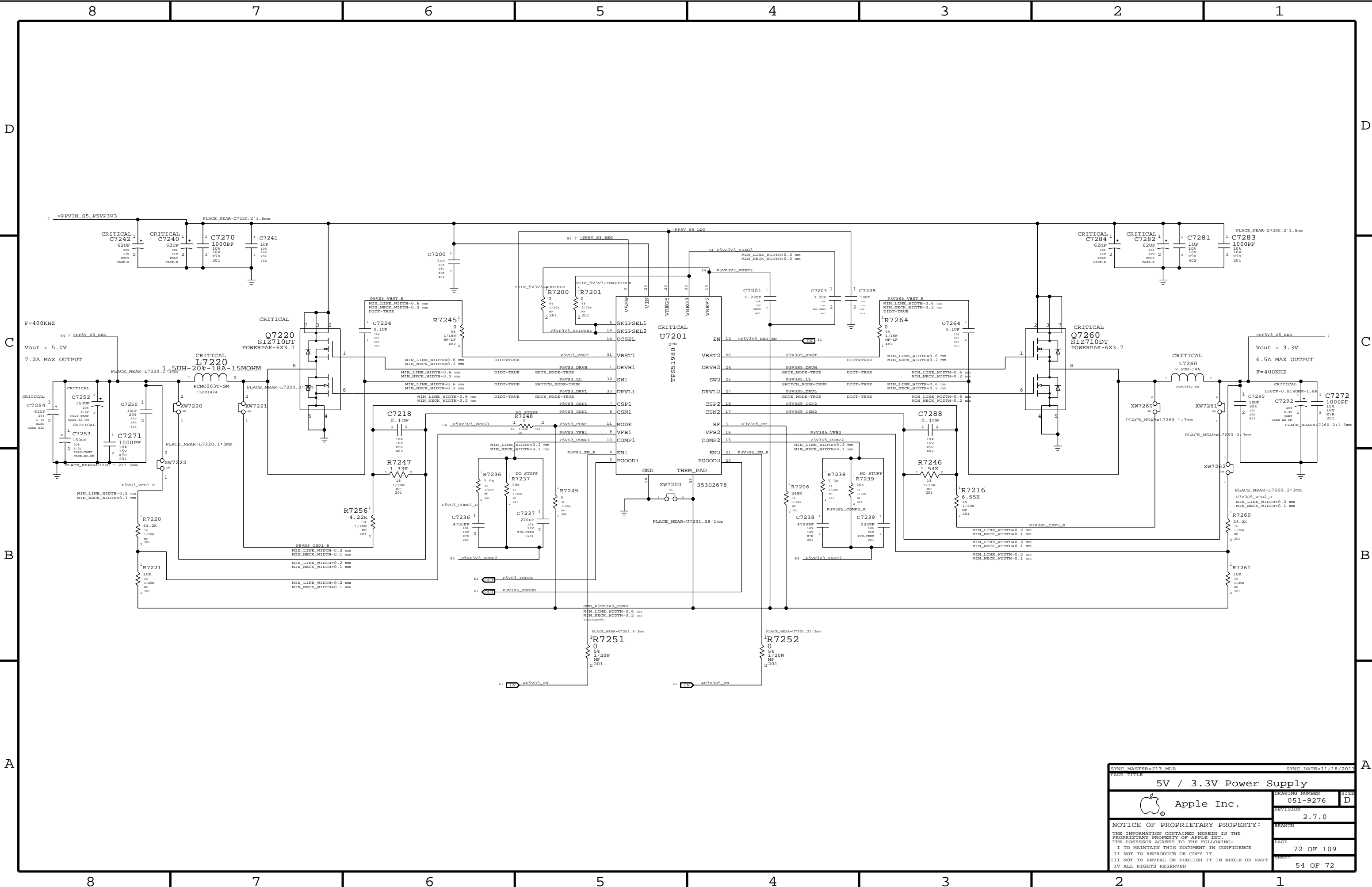



Right Speaker Connector

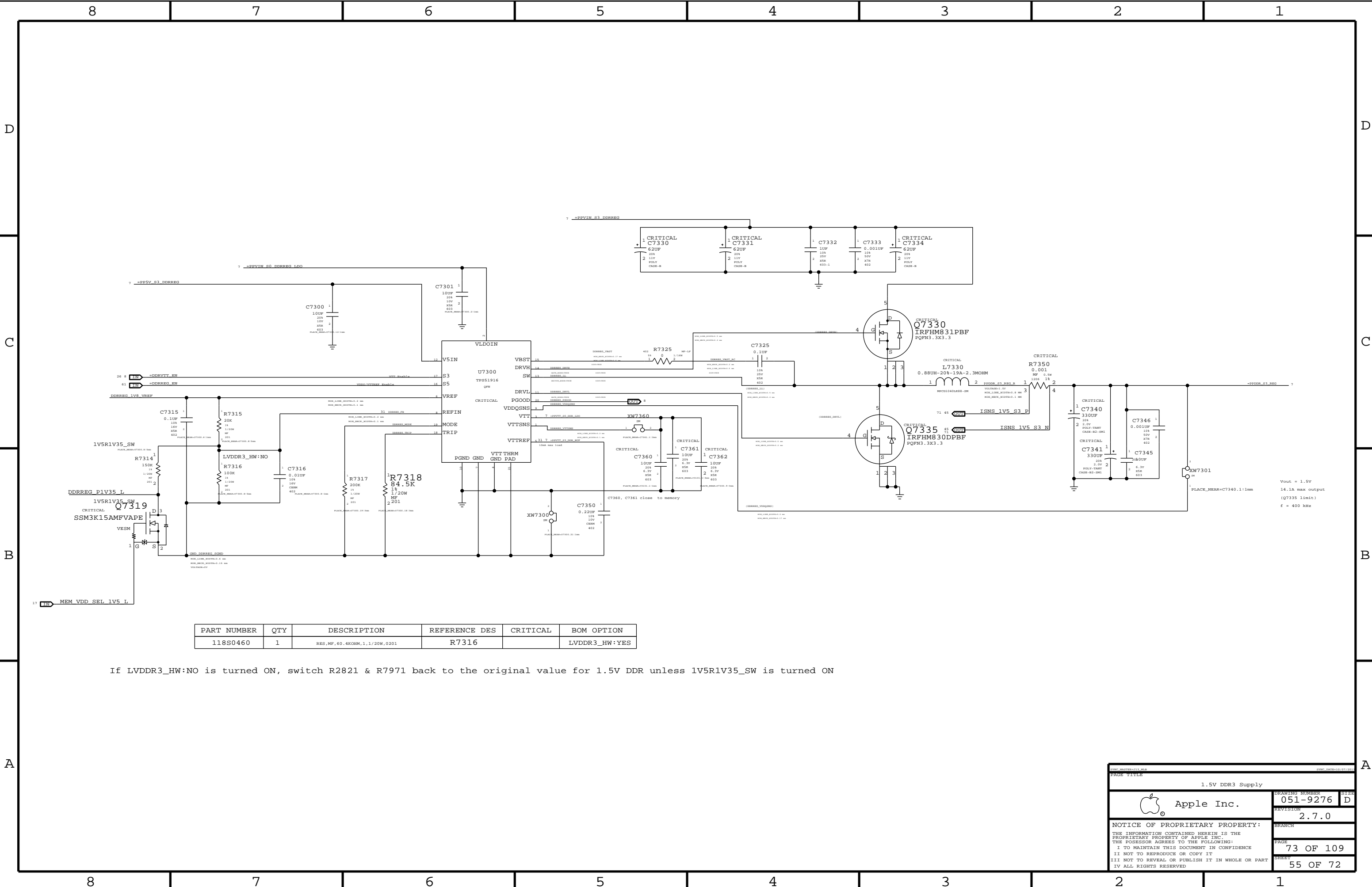


PAGE TITLE		DC-In & Battery Connectors	
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SYNC MASTER=J13 MLB		SYNC DATE=11/18/2011	
PAGE TITLE			
5V / 3.3V Power Supply			
 Apple Inc.		DRAWING NUMBER	051-9276
		SIZE	D
		REVISION	2.7.0
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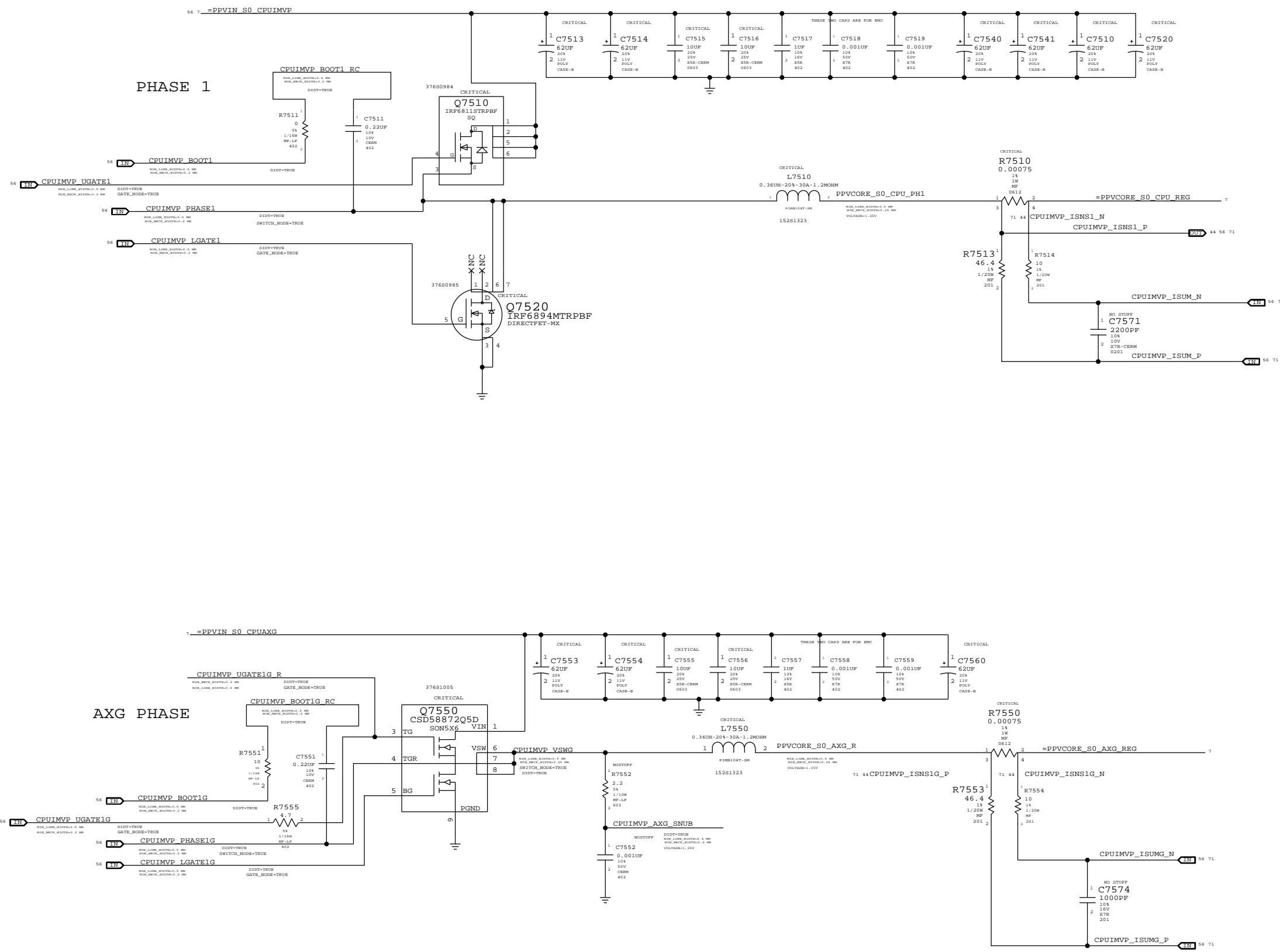
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0460	1	RES,MF,60.4KOHM,1,1/20W,0201	R7316		LVDDR3_HW:YES

If LVDDR3_HW:NO is turned ON, switch R2821 & R7971 back to the original value for 1.5V DDR unless 1V5R1V35_SW is turned ON

1.5V DDR3 Supply			
Apple Inc.		DRAWING NUMBER	051-9276
		REVISION	2.7.0
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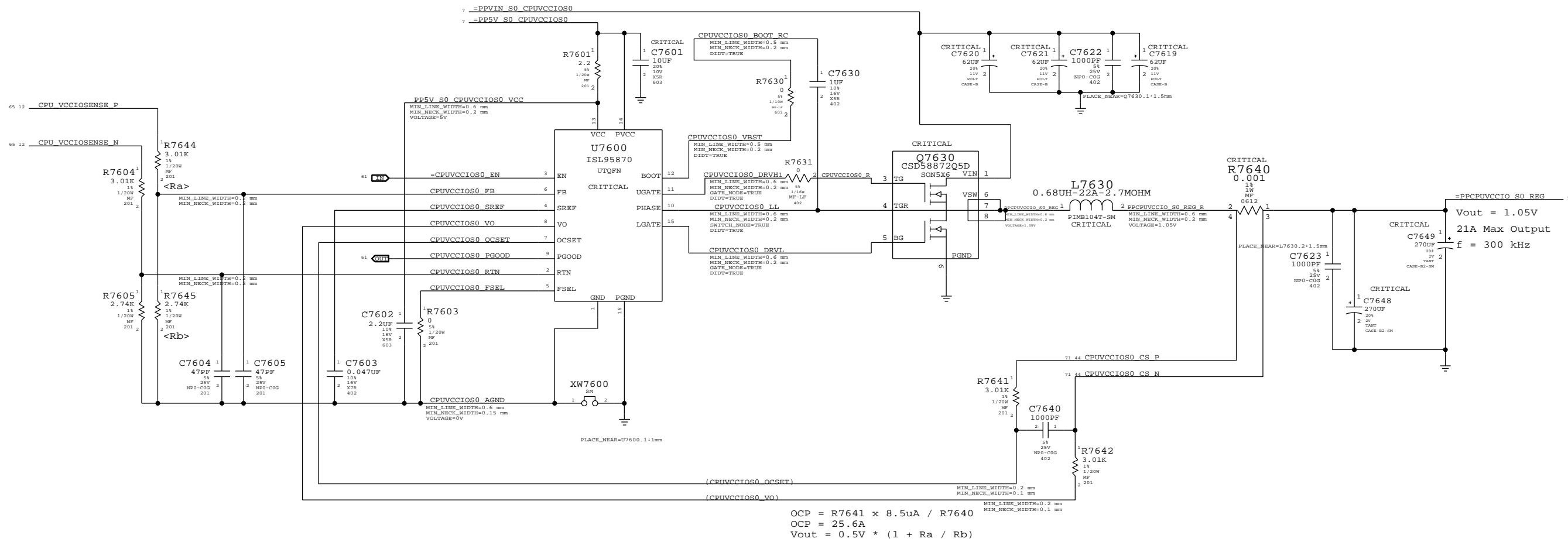


CPU=IV Bridge ULV, AXG=GT2



CPU IMVP7 & AXG VCore Output		
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	REVISION	2.7.0
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CPU VCCIO (1.05V S0) Regulator



$$OCP = R7641 \times 8.5\mu A / R7640$$
$$OCP = 25.6A$$
$$V_{out} = 0.5V \times (1 + R_a / R_b)$$

SYNOPSIS: CPU VCCIO (1.05V) Power Supply		SYNOPSIS: CPU VCCIO (1.05V) Power Supply
DRAWING NUMBER		051-9276
REVISION		2.7.0
BRANCH		
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D

C

B

A

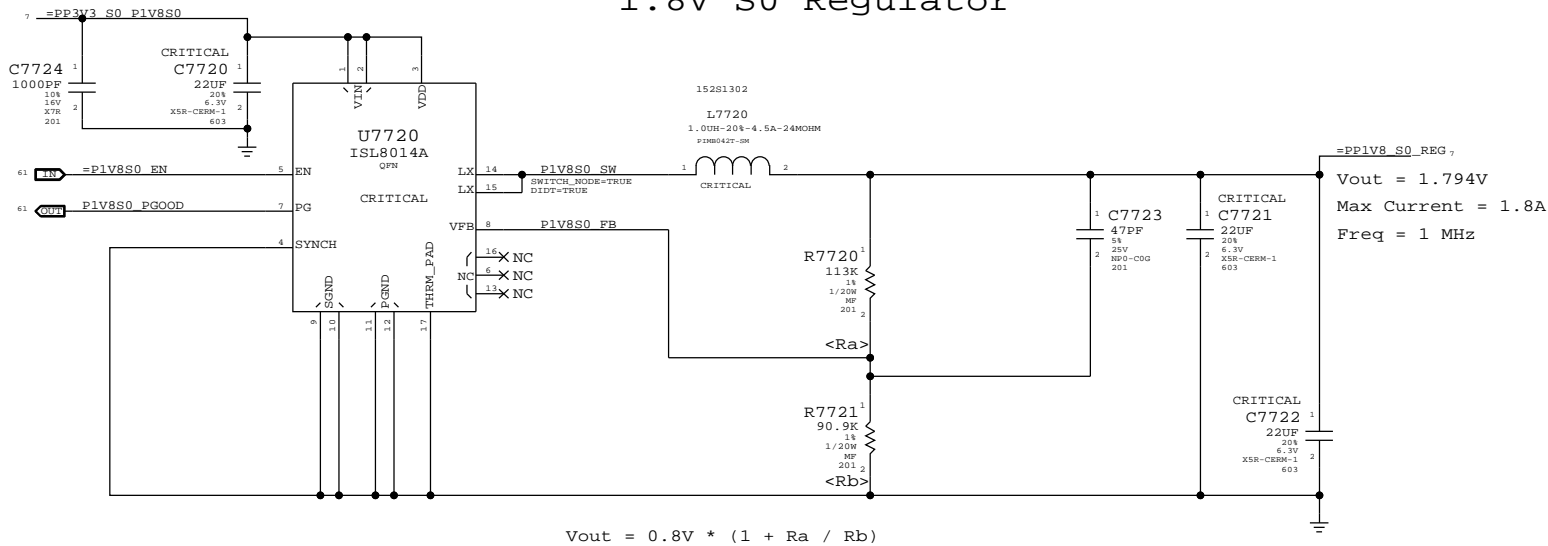
D

C

B

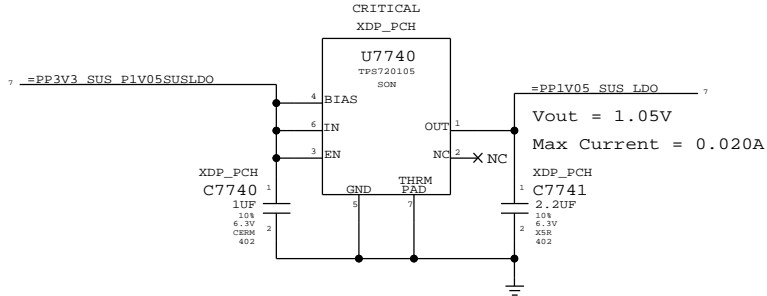
A

1.8V S0 Regulator

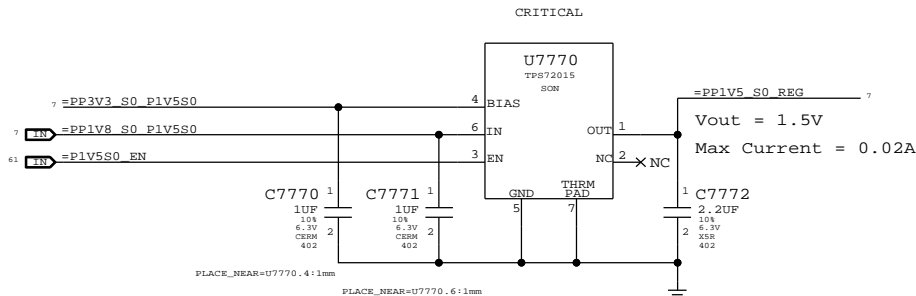


1.05V SUS LDO

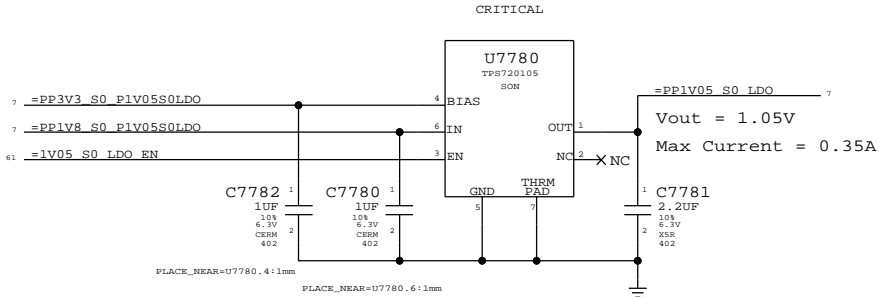
Cougar Point requires JTAG pull-ups to be powered at 1.05V when SUS suspend well is active. Pull-ups (3) must be 51 ohms to support XDP (not required in production). 70mA is required to support pull-ups. Alternative is strong voltage dividers (200/100) to 3.3V S5, which burns 100mW in all S-states.




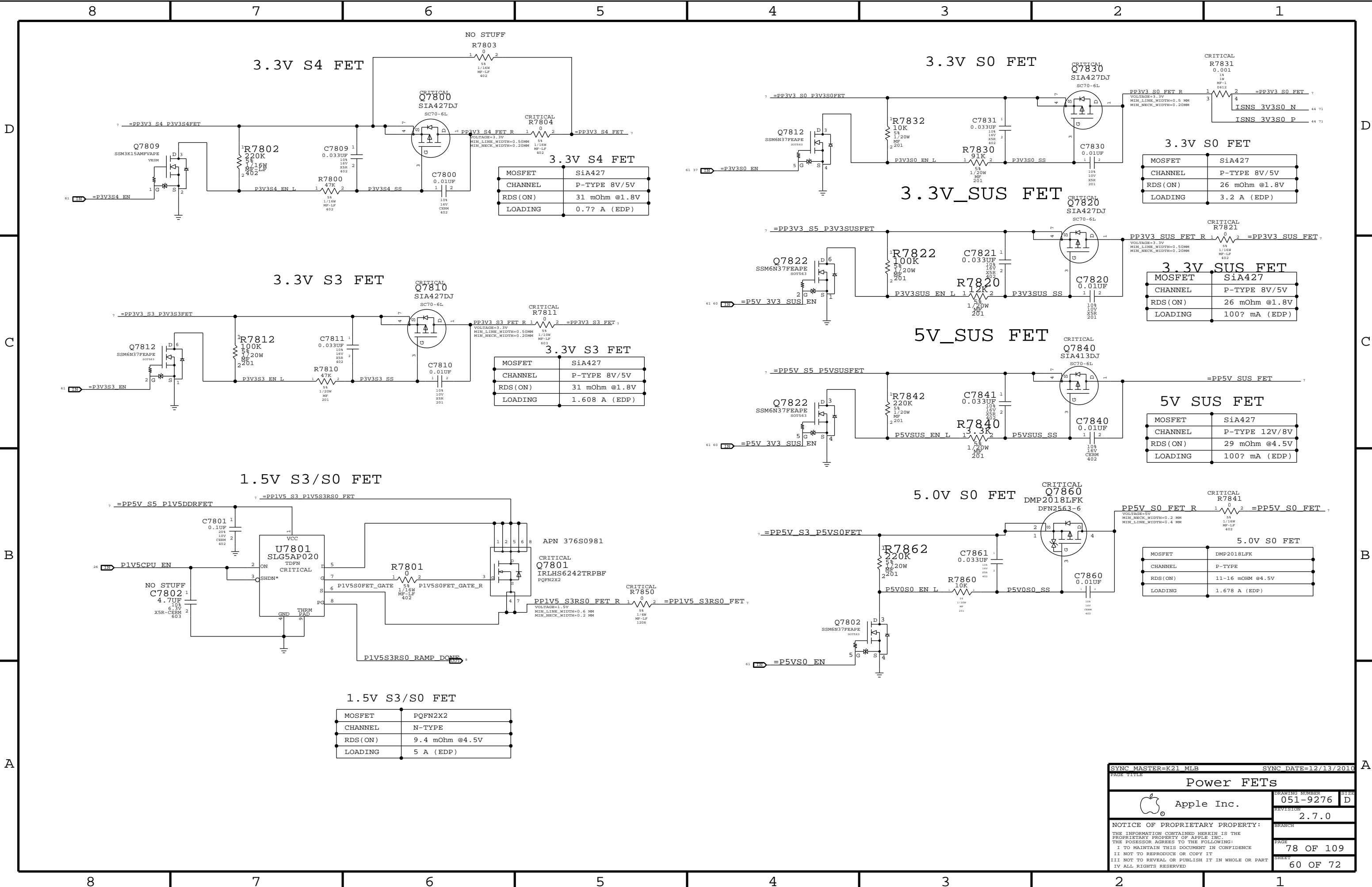
1.5V S0 LDO




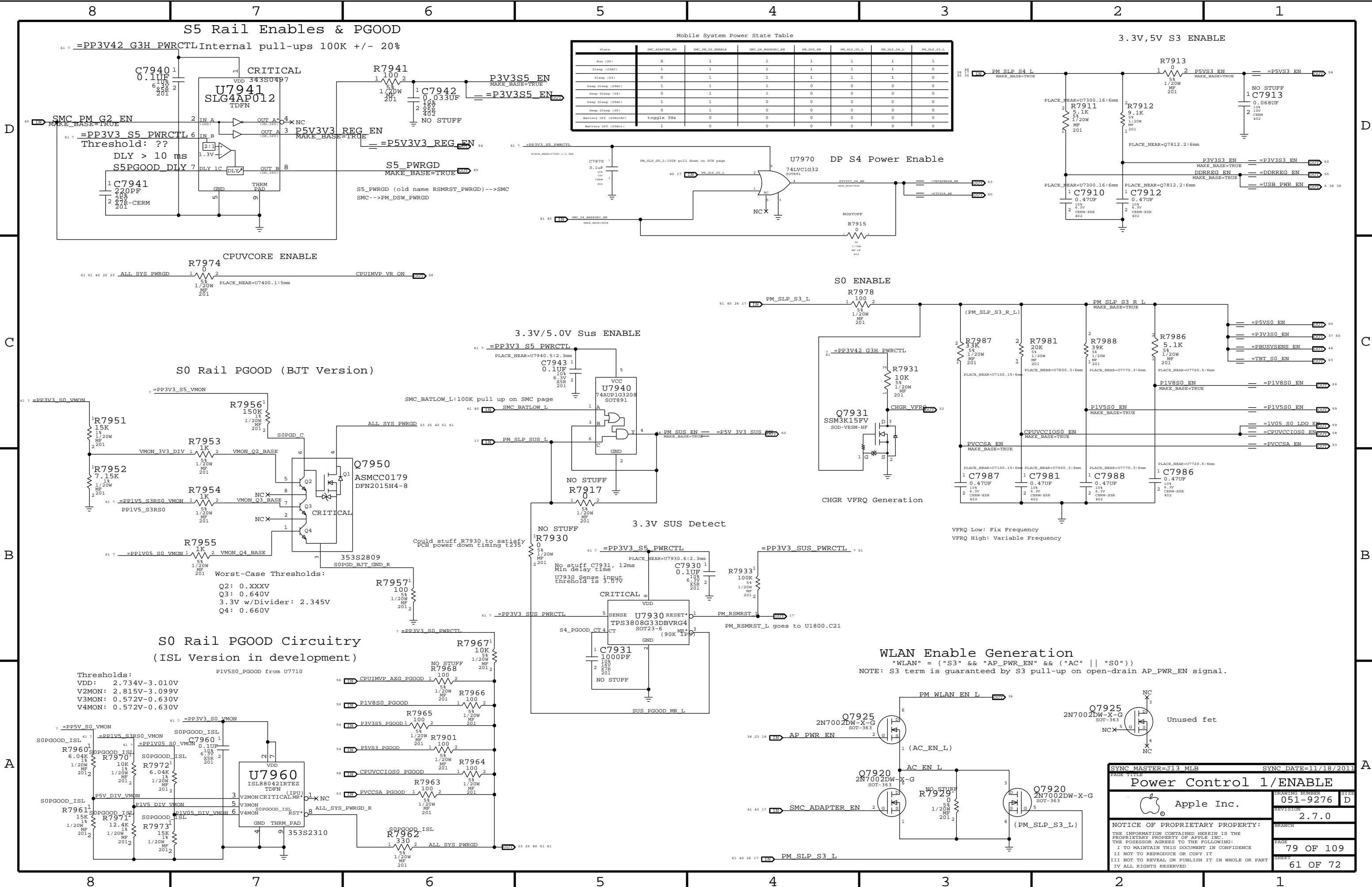
1.05V S0 LDO



SYNC MASTER=K21 MLB		SYNC DATE=12/13/2010	
PAGE TITLE			
Misc Power Supplies			
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PAGE TITLE			
Power FETs			
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	051-9276		D
	REVISION		
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State	SMC_ADAPTER_EN	SMC_PM_G2_ENABLE	SMC_S4_WAKEUP_EN	PM_SUS_EN	PM_SLP_S3_L	PM_SLP_S4_L	PM_SLP_S5_L
Run (S0)	X	1	1	1	1	1	1
Sleep (S3)	1	1	1	1	1	1	0
Deep Sleep (S4)	0	1	1	1	1	1	0
Deep Sleep (S4C)	1	1	1	0	0	0	0
Deep Sleep (S4C)	0	1	1	0	0	0	0
Deep Sleep (S5)	1	1	0	0	0	0	0
Battery Off (S5batt)	Toggle 3Hz	0	0	0	0	0	0
Battery Off (S5batt)	1	0	0	0	0	0	0

SYNC MASTER=J13 MLB

SYNC DATE=11/18/2011

Power Control 1/ENABLE

Apple Inc.

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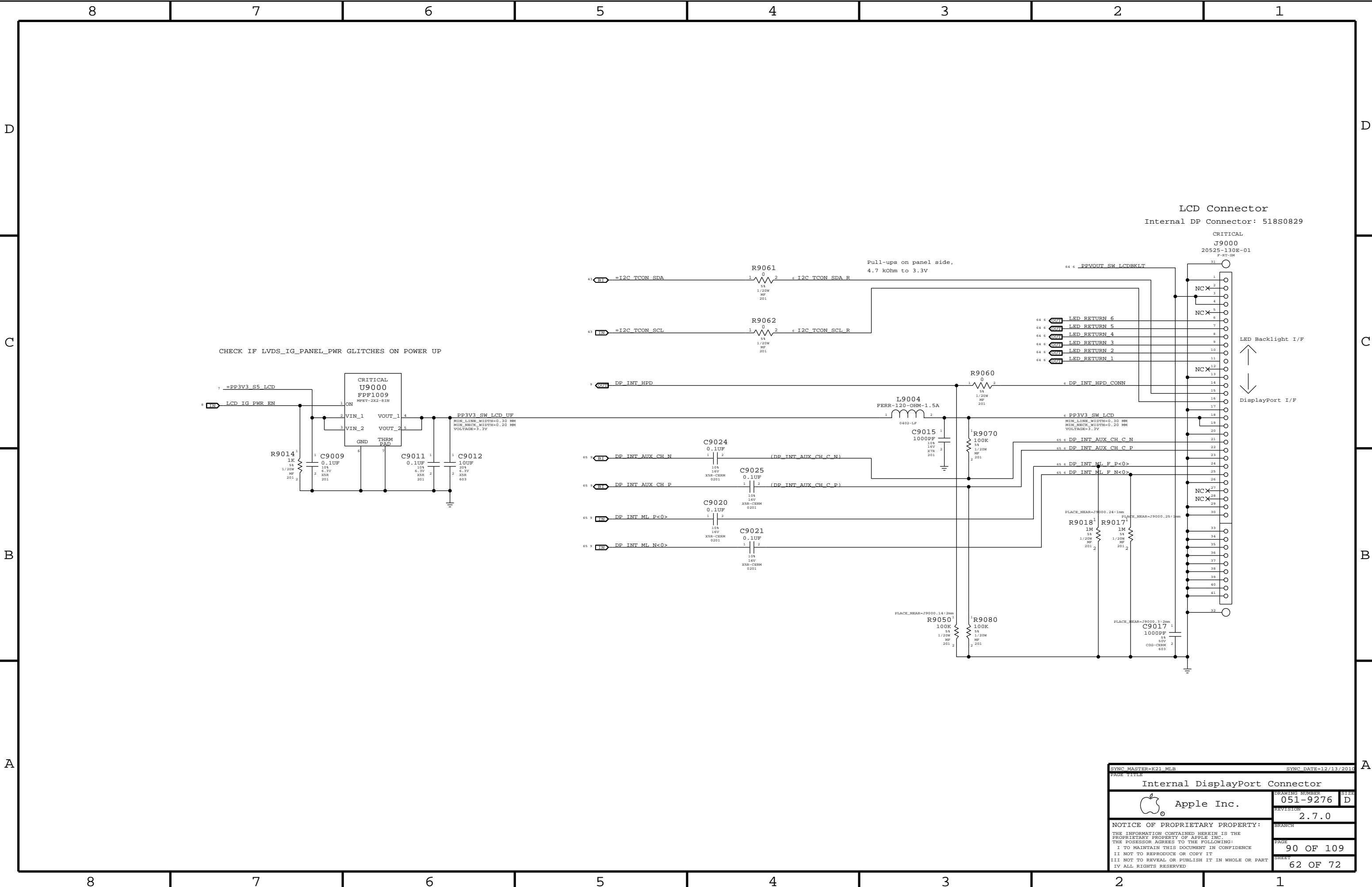
DRAWING NUMBER
051-9276


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SYNC MASTER=K21 MLB		SYNC DATE=12/13/2010	
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Internal DisplayPort Connector			
 Apple Inc.		DRAWING NUMBER	051-9276
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		REVISION	2.7.0
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8	7	6	5	4	3	2	1
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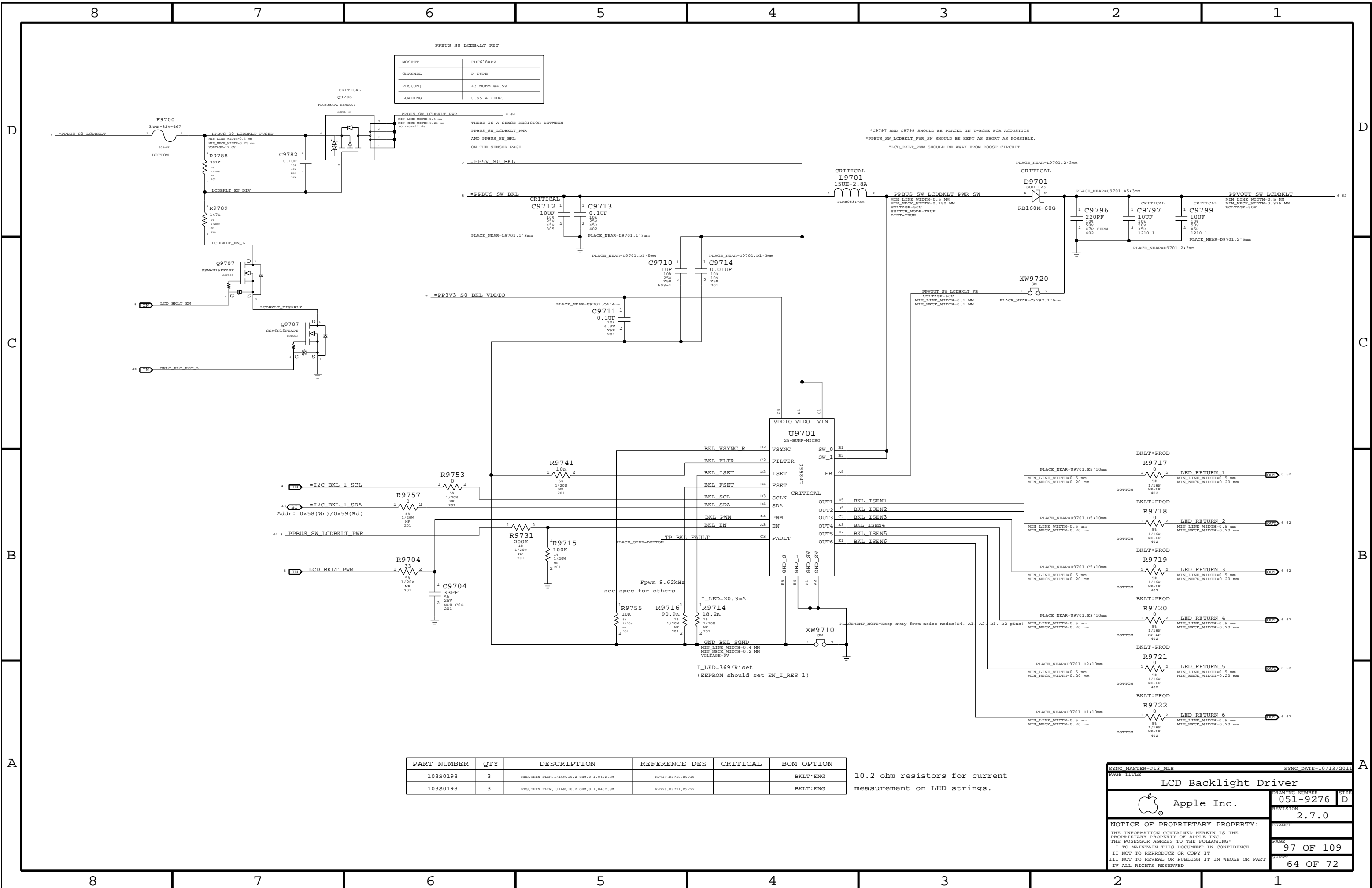
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0145	2	RES,MF,1/20W,17.8K,1.0201	R9410,R9413		TBTHV:P12V
118S0145	2	RES,MF,1/20W,17.8K,1.0201	R9411,R9414		TBTHV:P12V

B




8

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PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
103S0198	3	RES,THIN FILM,1/16W,10.2 OHM,0.1,0402,0H	R9717,R9718,R9719		BKLT:ENG
103S0198	3	RES,THIN FILM,1/16W,10.2 OHM,0.1,0402,0H	R9720,R9721,R9722		BKLT:ENG

10.2 ohm resistors for current measurement on LED strings.

SYNC MASTER=J13 MLB		SYNC DATE=10/13/2011	
PAGE TITLE			
LCD Backlight Driver			
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		SIZE	D
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SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA_ICOMP	*	=4x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SATA3_PCH_TX	SATA3_PCH_TX	*	SATA3_TX2TX
SATA3_PCH_RX	SATA3_PCH_RX	*	SATA3_RX2RX
SATA3_PCH_TX	*_PCH_TX	*	SATA3_TX2OTHERS
SATA3_PCH_RX	*_PCH_RX	*	SATA3_RX2OTHERS
SATA3_PCH_TX	*_PCH_RX	*	SATA3_TX2RX
SATA3_PCH_RX	*_PCH_TX	*	SATA3_RX2TX
SATA3_PCH_TX	*_TX	*	SATA3_2OTHERS
SATA3_PCH_RX	*_RX	*	SATA3_2OTHERS
SATA3_PCH_TX	*_RX	*	SATA3_2OTHERS
SATA3_PCH_RX	*	*	SATA3_2OTHER
SATA3_PCH_RX	*	*	SATA3_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA3_TX2TX	TOP,BOTTOM	=5x_DIELECTRIC	?
SATA3_RX2RX	TOP,BOTTOM	=5x_DIELECTRIC	?
SATA3_TX20THERTX	TOP,BOTTOM	=5x_DIELECTRIC	?
SATA3_RX20THERRX	TOP,BOTTOM	=5x_DIELECTRIC	?
SATA3_TX2RX	TOP,BOTTOM	=7x_DIELECTRIC	?
SATA3_RX2TX	TOP,BOTTOM	=7x_DIELECTRIC	?
SATA3_20THERHS	TOP,BOTTOM	=6x_DIELECTRIC	?
SATA3_20THER	TOP,BOTTOM	=5x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA3_TX2TX	*	= 2.5x_DIELECTRIC	?
SATA3_RX2RX	*	= 2.5x_DIELECTRIC	?
SATA3_TX2OTHERTX	*	= 4x_DIELECTRIC	?
SATA3_RX2OTHERRX	*	= 4x_DIELECTRIC	?
SATA3_TX2RX	*	= 6x_DIELECTRIC	?
SATA3_RX2TX	*	= 6x_DIELECTRIC	?
SATA3_20THERHS	*	= 4x_DIELECTRIC	?
SATA3_20THER	*	= 3x_DIELECTRIC	?

SOURCE: 471984_Chief_River_MS_PDG_1.0 and the spacing rule is adjusted per SI team feedback.

UART Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
UART_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
UART	*	=2x_DIELECTRIC	?

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_USB_RBIAS	*	=STANDARD	8 MIL	8 MIL	=STANDARD	=STANDARD	=STANDARD
USB_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=2x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for Ibex Peak M (DG-398905-398905_v1.5), Section 3.8

USB 3.0 Interface Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
USB3_PCH_TX	USB3_PCH_TX	*	USB3_TX2TX
USB3_PCH_RX	USB3_PCH_RX	*	USB3_RX2RX
USB3_PCH_TX	*_PCH_TX	*	USB3_TX2OTHERTX
USB3_PCH_RX	*_PCH_RX	*	USB3_RX2OTHERRX
USB3_PCH_TX	*_PCH_RX	*	USB3_TX2RX
USB3_PCH_RX	*_PCH_TX	*	USB3_RX2TX
USB3_PCH_TX	*_TX	*	USB3_2OTHERHS
USB3_PCH_RX	*_TX	*	USB3_2OTHERHS
USB3_PCH_TX	*_RX	*	USB3_2OTHERHS
USB3_PCH_RX	*_RX	*	USB3_2OTHERHS
USB3_PCH_TX	*	*	USB3_2OTHER
USB3_PCH_RX	*	*	USB3_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3_TX2TX	TOP,BOTTOM	=5x_DIELECTRIC	?
USB3_RX2RX	TOP,BOTTOM	=5x_DIELECTRIC	?
USB3_TX2TOTHERTX	TOP,BOTTOM	=5x_DIELECTRIC	?
USB3_RX2TOTHERRX	TOP,BOTTOM	=5x_DIELECTRIC	?
USB3_TX2RX	TOP,BOTTOM	=7x_DIELECTRIC	?
USB3_RX2TX	TOP,BOTTOM	=7x_DIELECTRIC	?
USB3_2OTHERHS	TOP,BOTTOM	=6x_DIELECTRIC	?
USB3_2OTHERS	TOP,BOTTOM	=5x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3_TX2TX	*	= 2.5x_DIELECTRIC	?
USB3_RX2RX	*	= 2.5x_DIELECTRIC	?
USB3_TX20THERTX	*	= 4x_DIELECTRIC	?
USB3_RX20THERRX	*	= 4x_DIELECTRIC	?
USB3_TX2RX	*	= 6x_DIELECTRIC	?
USB3_RX2TX	*	= 6x_DIELECTRIC	?
USB3_20THERHS	*	= 4x_DIELECTRIC	?
USB3_20THER	*	= 3x_DIELECTRIC	?

SOURCE: 471984_Cheif_River_MS_PDG_1.0 and the spacing rule is adjusted per SI team feedback.

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET		NET_TYPE			
		PHYSICAL	SPACING		
[]	SATA_PCH_MUX_R2D	SATA_80D	SATA3_PCH_TX	SATA_HDD_R2D_C_P	16 37
	SATA_PCH_MUX_R2D	SATA_80D	SATA3_PCH_TX	SATA_HDD_R2D_C_N	16 37
[]		SATA_80D	SATA3_PCH_TX	SATA_SSD_R2D_MUX_IN_P	37
		SATA_80D	SATA3_PCH_TX	SATA_SSD_R2D_MUX_IN_N	37
[]	SATA_MUX_SSD_R2D	SATA_80D	SATA3_PCH_TX	SATA_SSD_R2D_P	6 37
	SATA_MUX_SSD_R2D	SATA_80D	SATA3_PCH_TX	SATA_SSD_R2D_N	6 37
[]	SATA_PCH_MUX_D2R	SATA_80D	SATA3_PCH_RX	SATA_HDD_D2R_P	16 37
	SATA_PCH_MUX_D2R	SATA_80D	SATA3_PCH_RX	SATA_HDD_D2R_N	16 37
[]		SATA_80D	SATA3_PCH_RX	SATA_SSD_D2R_MUX_OUT_P	37
		SATA_80D	SATA3_PCH_RX	SATA_SSD_D2R_MUX_OUT_N	37
[]	SATA_MUX_SSD_D2R	SATA_80D	SATA3_PCH_RX	SATA_SSD_D2R_P	6 37
	SATA_MUX_SSD_D2R	SATA_80D	SATA3_PCH_RX	SATA_SSD_D2R_N	6 37
[]	PCH_SATA_ICOMP		SATA_ICOMP	PCH_SATAICOMP	16
[]	USB_HUB1_UP	USB_80D	USB	USB_HUB_UP_P	18 24
	USB_HUB1_UP	USB_80D	USB	USB_HUB_UP_N	18 24
[]	USB_BT	USB_80D	USB	USB_BT_P	24 36
	USB_BT	USB_80D	USB	USB_BT_N	24 36
[]		USB_80D	USB	USB_BT_CONN_P	6 36
		USB_80D	USB	USB_BT_CONN_N	6 36
[]		USB_80D	USB	USB_BT_WAKE_P	36
		USB_80D	USB	USB_BT_WAKE_N	36
[]	USB_TP4D	USB_80D	USB	USB_TP4D_P	6 48
	USB_TP4D	USB_80D	USB	USB_TP4D_N	6 48
[]		USB_80D	USB	USB_TP4D_CONN_P	
		USB_80D	USB	USB_TP4D_CONN_N	
[]	USB_TP4D_HUB	USB_80D	USB	USB_TP4D_HUB_P	24
	USB_TP4D_HUB	USB_80D	USB	USB_TP4D_HUB_N	24
[]		USB_80D	USB	USB_TP4D_R_P	24 48
		USB_80D	USB	USB_TP4D_R_N	24 48
[]	USB_TP4D_M	USB_80D	USB	USB_TP4D_M_P	48
	USB_TP4D_M	USB_80D	USB	USB_TP4D_M_N	48
[]	USB_SDCARD	USB_80D	USB	USB_SDCARD_P	8 24
	USB_SDCARD	USB_80D	USB	USB_SDCARD_N	8 24
[]	USB_SMC	USB_80D	USB	USB_SMC_P	24 40
	USB_SMC	USB_80D	USB	USB_SMC_N	24 40
[]	USB_CAMERA	USB_80D	USB	USB_CAMERA_P	6 18 39
	USB_CAMERA	USB_80D	USB	USB_CAMERA_N	6 18 39
[]	USB_EXT4	USB_80D	USB	USB_EXT4_P	18 38
	USB_EXT4	USB_80D	USB	USB_EXT4_N	18 38
[]		UART_45S	UART	SMC_DEBUGPRT_TX_L	38 40 41
		UART_45S	UART	SMC_DEBUGPRT_RX_L	38 40 41
[]		USB_80D	USB	USB2_EXT4_MUXED_P	38
		USB_80D	USB	USB2_EXT4_MUXED_N	38
[]		USB_80D	USB	USB2_EXT4_MUXED_F_P	38
		USB_80D	USB	USB2_EXT4_MUXED_F_N	38
[]	USB3_EXT4_RX	USB_80D	USB3_PCH_RX	USB3_EXT4_RX_P	18 38
	USB3_EXT4_RX	USB_80D	USB3_PCH_RX	USB3_EXT4_RX_N	18 38
[]	USB3_EXT4_TX	USB_80D	USB3_PCH_TX	USB3_EXT4_TX_P	18 38
	USB3_EXT4_TX	USB_80D	USB3_PCH_TX	USB3_EXT4_TX_N	18 38
[]		USB_80D	USB3_PCH_RX	USB3_EXT4_RX_F_P	38
		USB_80D	USB3_PCH_RX	USB3_EXT4_RX_F_N	38
[]		USB_80D	USB3_PCH_TX	USB3_EXT4_TX_F_P	38
		USB_80D	USB3_PCH_TX	USB3_EXT4_TX_F_N	38
[]		USB_80D	USB3_PCH_TX	USB3_EXT4_TX_C_P	38
		USB_80D	USB3_PCH_TX	USB3_EXT4_TX_C_N	38
[]	USB_EXTB	USB_80D	USB	USB_EXTB_P	6 24 39
	USB_EXTB	USB_80D	USB	USB_EXTB_N	6 24 39
[]		USB_80D	USB	USB_EXTB_EHCI_P	18 24
		USB_80D	USB	USB_EXTB_EHCI_N	18 24
[]		USB_80D	USB	USB_EXTB_XHCI_P	18 24
		USB_80D	USB	USB_EXTB_XHCI_N	18 24
[]	USB3_EXTB_RX	USB_80D	USB3_PCH_RX	USB3_EXTB_RX_P	18 39
	USB3_EXTB_RX	USB_80D	USB3_PCH_RX	USB3_EXTB_RX_N	18 39
[]		USB_80D	USB3_PCH_RX	USB3_EXTB_RX_RC_P	6 39
		USB_80D	USB3_PCH_RX	USB3_EXTB_RX_RC_N	6 39
[]		USB_80D	USB3_PCH_RX	USB3_EXTB_RX_CONN_P	
		USB_80D	USB3_PCH_RX	USB3_EXTB_RX_CONN_N	
[]	USB3_EXTB_TX	USB_80D	USB3_PCH_TX	USB3_EXTB_TX_P	18 39
	USB3_EXTB_TX	USB_80D	USB3_PCH_TX	USB3_EXTB_TX_N	18 39
[]		USB_80D	USB3_PCH_TX	USB3_EXTB_TX_C_P	6 39
		USB_80D	USB3_PCH_TX	USB3_EXTB_TX_C_N	6 39
[]	(USB_TP4D_HUB)	USB_80D	USB	USB_EXTD_XHCI_P	18 24
	(USB_TP4D_HUB)	USB_80D	USB	USB_EXTD_XHCI_N	18 24
[]	PCH_USB_RBIAS	PCH_USB_RBIAS		PCH_USB_RBIAS	18
	PCH_DIFCLK_UNUSED	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_PCH_P	16
[]	PCH_DIFCLK_UNUSED	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_PCH_N	16
	PCH_DIFCLK_UNUSED	CLK_PCIE_80D	CLK_PCIE	PCH_CLK96M_DOT_P	16
[]	PCH_DIFCLK_UNUSED	CLK_PCIE_80D	CLK_PCIE	PCH_CLK96M_DOT_N	16
	PCH_DIFCLK_UNUSED	CLK_PCIE_80D	CLK_PCIE	PCH_CLK100M_SATA_P	16
[]	PCH_DIFCLK_UNUSED	CLK_PCIE_80D	CLK_PCIE	PCH_CLK100M_SATA_N	16
	PCH_DIFCLK_UNUSED	CPU_45S	CLK_PCIE	PCH_CLK14P3M_REFCLK	16

SATA SSD


USB Hub nets

USB Camera nets

USB EXTA nets (Right USB port)

USB EXTB nets (Left USB port)

Unused USB nets

SYNC MASTER=CONSTRAINTS		SYNC DATE=01/11/2012	
PAGE TITLE			
PCH Constraints 1			
	Apple Inc.	DRAWING NUMBER	051-9276
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LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	=3x_DIELECTRIC	?
CLK_LPC	*	=4x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for Ixex Peak M (DG-398905-398905_v1.5), Section 3.15

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_45S_R_50S	TOP,BOTTOM	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE		
SMB_45S_R_50S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for Ixex Peak M (DG-398905-398905_v1.5), Section 3.15

SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	=4x_DIELECTRIC	?

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	=4x_DIELECTRIC	?

XDP Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCH_ITP	*	=2:1_SPACING	?

DisplayPort

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DP_2DP	*	=3x_DIELECTRIC	?
DP_2OTHERHS	*	=4x_DIELECTRIC	?
DP_2OTHER	*	=3x_DIELECTRIC	?
DP_AUX	*	=3x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DP_TX	DP_TX	*	DP_2DP
DP_TX	*_TX	*	DP_2OTHERHS
DP_TX	*_RX	*	DP_2OTHERHS
DP_TX	*	*	DP_2OTHER

System Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CLK_25M_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

















SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	=2x_DIELECTRIC	?
CLK_25M	*	=5x_DIELECTRIC	?

NOTE: 25MHz system clocks very sensitive to noise.









PCH Net Properties

ELECTRICAL_CONSTRAINT_SET		NET_TYPE		
		PHYSICAL	SPACING	
	LPC_AD	LPC_45S	LPC	LPC_AD<3..0>
	LPC_FRAME_L	LPC_45S	LPC	LPC_FRAME_L
		LPC_45S	LPC	LPCPLUS RESET_L
	LPC_CLK33M	CLK LPC_45S	CLK LPC	LPC_CLK33M_SMC
		CLK LPC_45S	CLK LPC	LPC_CLK33M_SMC_R
	LPC_CLK33M	CLK LPC_45S	CLK LPC	LPC_CLK33M_LPCPLUS
		CLK LPC_45S	CLK LPC	LPC_CLK33M_LPCPLUS_R
	LPC_CLK33M	CLK LPC_45S	CLK LPC	PCH_CLK33M_PCIIN
		CLK LPC_45S	CLK LPC	PCH_CLK33M_PCIOUT
	SMBUS_PCH_CLK	SMB_45S_R_50S	SMB	SMBUS_PCH_CLK
	SMBUS_PCH_DATA	SMB_45S_R_50S	SMB	SMBUS_PCH_DATA
	SMBUS_PCH_0_CLK	SMB_45S_R_50S	SMB	SML_PCH_0_CLK
	SMBUS_PCH_0_DATA	SMB_45S_R_50S	SMB	SML_PCH_0_DATA
	SMBUS_SMC_1_S0_SCL	SMB_45S_R_50S	SMB	SML_PCH_1_CLK
	SMBUS_SMC_1_S0_SDA	SMB_45S_R_50S	SMB	SML_PCH_1_DATA
	HDA_BIT_CLK	HDA_45S	HDA	HDA_BIT_CLK
		HDA_45S	HDA	HDA_BIT_CLK_R
	HDA_SYNC	HDA_45S	HDA	HDA_SYNC
		HDA_45S	HDA	HDA_SYNC_R
	HDA_RST_L	HDA_45S	HDA	HDA_RST_R_L
		HDA_45S	HDA	HDA_RST_L
	HDA_SDIN0	HDA_45S	HDA	HDA_SDIN0
	HDA_SDOUT	HDA_45S	HDA	HDA_SDOUT
		HDA_45S	HDA	HDA_SDOUT_R
	PM_SUS_CLK	CLK_SLOW_45S	CLK_SLOW	PM_CLK32K_SUSCLK_R
		CLK_SLOW_45S	CLK_SLOW	SMC_CLK32K
	SPI_CLK	SPI_45S	SPI	SPI_CLK_R
		SPI_45S	SPI	SPI_CLK
	SPI_MOSI	SPI_45S	SPI	SPI_MOSI_R
		SPI_45S	SPI	SPI_MOSI
	SPI_MISO	SPI_45S	SPI	SPI_MISO
	SPI_CS0	SPI_45S	SPI	SPI_CS0_R_L
		SPI_45S	SPI	SPI_CS0_L
		SPI_45S	SPI	SPI_SMC_CLK
		SPI_45S	SPI	SPI_SMC_MOSI
		SPI_45S	SPI	SPI_SMC_MISO
		SPI_45S	SPI	SPI_SMC_CS_L
		SPI_45S	SPI	SPI_MLB_CLK
		SPI_45S	SPI	SPI_MLB_MOSI
		SPI_45S	SPI	SPI_MLB_MISO
		SPI_45S	SPI	SPI_MLB_CS_L
	PCIE_AP_R2D	PCIE_80D	PCIE_PCH_TX	PCIE_AP_R2D_P
	PCIE_AP_R2D	PCIE_80D	PCIE_PCH_TX	PCIE_AP_R2D_N
		PCIE_80D	PCIE_PCH_TX	PCIE_AP_R2D_C_P
		PCIE_80D	PCIE_PCH_TX	PCIE_AP_R2D_C_N
	PCIE_AP_D2R	PCIE_80D	PCIE_PCH_RX	PCIE_AP_D2R_P
	PCIE_AP_D2R	PCIE_80D	PCIE_PCH_RX	PCIE_AP_D2R_N
	PCIE_CLK100M_AP	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_AP_P
	PCIE_CLK100M_AP	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_AP_N
	PCIE_TBT_R2D	PCIE_80D	PCIE_PCH_TX	PCIE_TBT_R2D_P<3..0>
	PCIE_TBT_R2D	PCIE_80D	PCIE_PCH_TX	PCIE_TBT_R2D_N<3..0>
		PCIE_80D	PCIE_PCH_TX	PCIE_TBT_R2D_C_P<3..0>
		PCIE_80D	PCIE_PCH_TX	PCIE_TBT_R2D_C_N<3..0>
	PCIE_TBT_D2R	PCIE_80D	PCIE_PCH_RX	PCIE_TBT_D2R_P<3..0>
	PCIE_TBT_D2R	PCIE_80D	PCIE_PCH_RX	PCIE_TBT_D2R_N<3..0>
		PCIE_80D	PCIE_PCH_RX	PCIE_TBT_D2R_C_P<3..0>
		PCIE_80D	PCIE_PCH_RX	PCIE_TBT_D2R_C_N<3..0>
	PCIE_CLK100M_TBT	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_TBT_P
	PCIE_CLK100M_TBT	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_TBT_N
		CLK_PCIE_80D	CLK_PCIE	PEG_CLK100M_P
		CLK_PCIE_80D	CLK_PCIE	PEG_CLK100M_N
	XDP_TDI	PCH_45S	PCH_TTP	XDP_PCH_TDI
	XDP_TDO	PCH_45S	PCH_TTP	XDP_PCH_TDO
	XDP_TMS	PCH_45S	PCH_TTP	XDP_PCH_TMS
	XDP_TCK	PCH_45S	PCH_TTP	XDP_PCH_TCK

Chipset Net Properties

ELECTRICAL_CONSTRAINT_SET		NET_TYPE		
		PHYSICAL	SPACING	
	DP_TBT_ML	DP_80D	DP_TX	DP TBTSNK0 ML P<3..0>
	DP_TBT_ML	DP_80D	DP_TX	DP TBTSNK0 ML N<3..0>
		DP_80D	DP_TX	DP TBTSNK0 ML C P<3..0>
		DP_80D	DP_TX	DP TBTSNK0 ML C N<3..0>
	DP_TBT_AUXCH	DP_80D	DP_AUX	DP TBTSNK0 AUXCH P
	DP_TBT_AUXCH	DP_80D	DP_AUX	DP TBTSNK0 AUXCH N
		DP_80D	DP_AUX	DP TBTSNK0 AUXCH C P
		DP_80D	DP_AUX	DP TBTSNK0 AUXCH C N
	DP_TBT_ML	DP_80D	DP_TX	DP TBTSNK1 ML P<3..0>
	DP_TBT_ML	DP_80D	DP_TX	DP TBTSNK1 ML N<3..0>
		DP_80D	DP_TX	DP TBTSNK1 ML C P<3..0>
		DP_80D	DP_TX	DP TBTSNK1 ML C N<3..0>
	DP_TBT_AUXCH	DP_80D	DP_AUX	DP TBTSNK1 AUXCH P
	DP_TBT_AUXCH	DP_80D	DP_AUX	DP TBTSNK1 AUXCH N
		DP_80D	DP_AUX	DP TBTSNK1 AUXCH C P
		DP_80D	DP_AUX	DP TBTSNK1 AUXCH C N

Clock Net Properties

ELECTRICAL_CONSTRAINT_SET		NET_TYPE			
		PHYSICAL	SPACING		
	SYSCLK_CLK32K_RTC	CLK_SLOW_45S	CLK_SLOW	SYSCLK_CLK32K_RTC	16 25
	SYSCLK_CLK25M_SB	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_SB	16 25
		CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_SB_R	16
	SYSCLK_CLK25M_TBT	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_TBT	25 33
		CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_TBT_R	33
	SYSCLK_CLK25M_XTAL	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_X1	25
		CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_X2	25
		CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_X2_R	25

Thunderbolt IC Net Properties

Only used on hosts supporting Thunderbolt video-in

87654321

Thunderbolt Constraints

Apple Inc.

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